Compal Confidential

2014 S-series(400series) Rolo/Reeses/Raisinet

INTEL Sharkbay & Crescent bay ULT –U processor with DDR3L

Date : 2014/02/18

Version 0.5

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Title: Cover Page		
Size: B	Document Number: LA-B181P	Rev: 0.5
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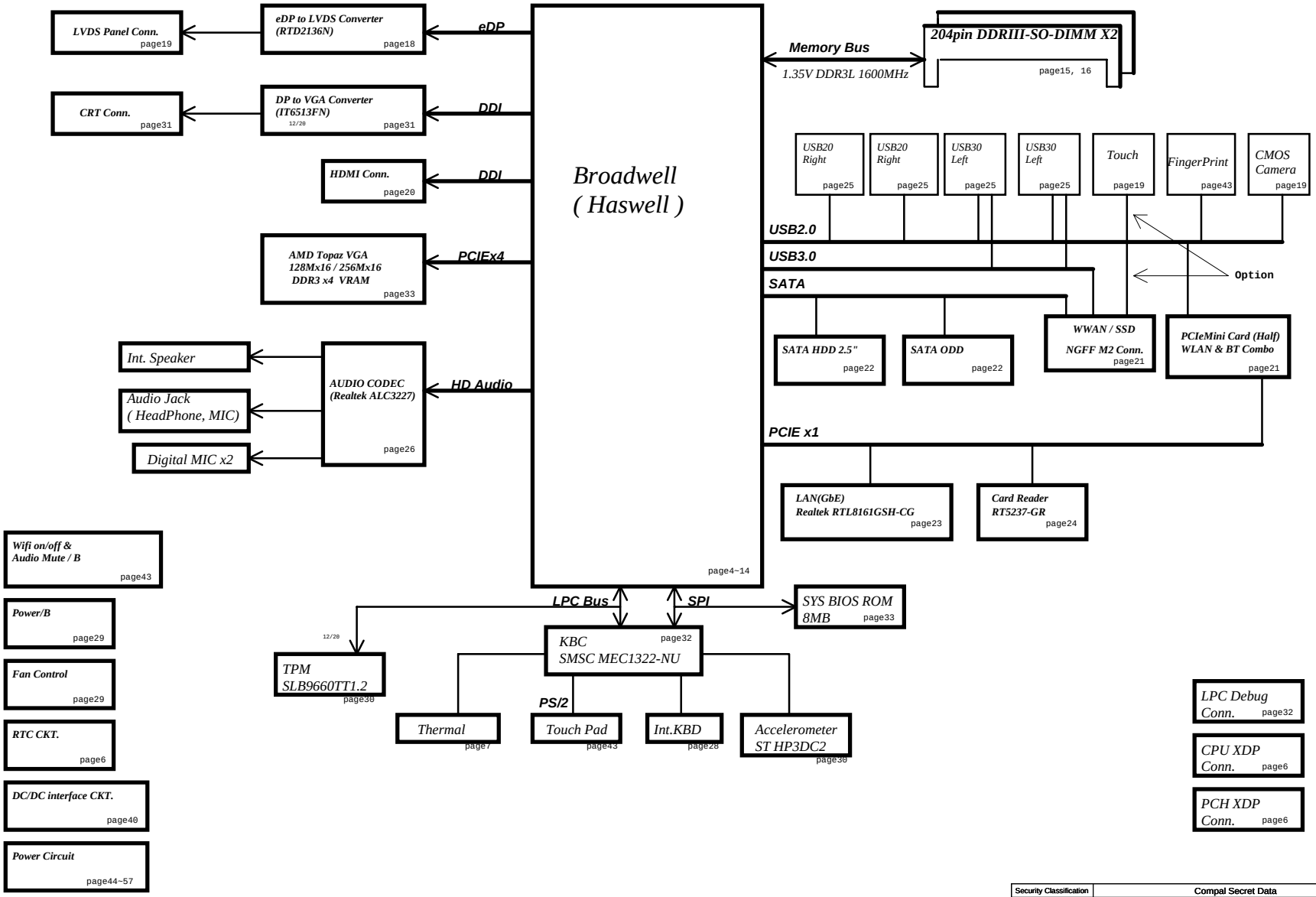
Compal Confidential

Model Name :

Intel Broadwell U / Haswell Block Diagram

Project Name :



CPU DC/DC TPS51622ARSMR 50~51	
INPUTS	OUTPUTS
B+	VCC_VORE

SYSTEM DC/DC RT8243AZQW 47	
INPUTS	OUTPUTS
B+	3VDS/5VDS

SYSTEM DC/DC RT8207MZQW 48	
INPUTS	OUTPUTS
B+	1.35V_VDDQ 0.675VS

SYSTEM DC/DC SY8206DQNC 49	
INPUTS	OUTPUTS
B+	1.05VS

SYSTEM DC/DC SY8003DFC 52	
INPUTS	OUTPUTS
B+	1.5VS

SYSTEM DC/DC RT8880BGQW 54~55	
INPUTS	OUTPUTS
B+	+VGA_CORE

SYSTEM DC/DC SY8003DFC 56	
INPUTS	OUTPUTS
B+	+1.8VS_VGA

SYSTEM DC/DC SY8003DFC 57	
INPUTS	OUTPUTS
B+	+0.95VS_VGA

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Title	Block Diagrams		
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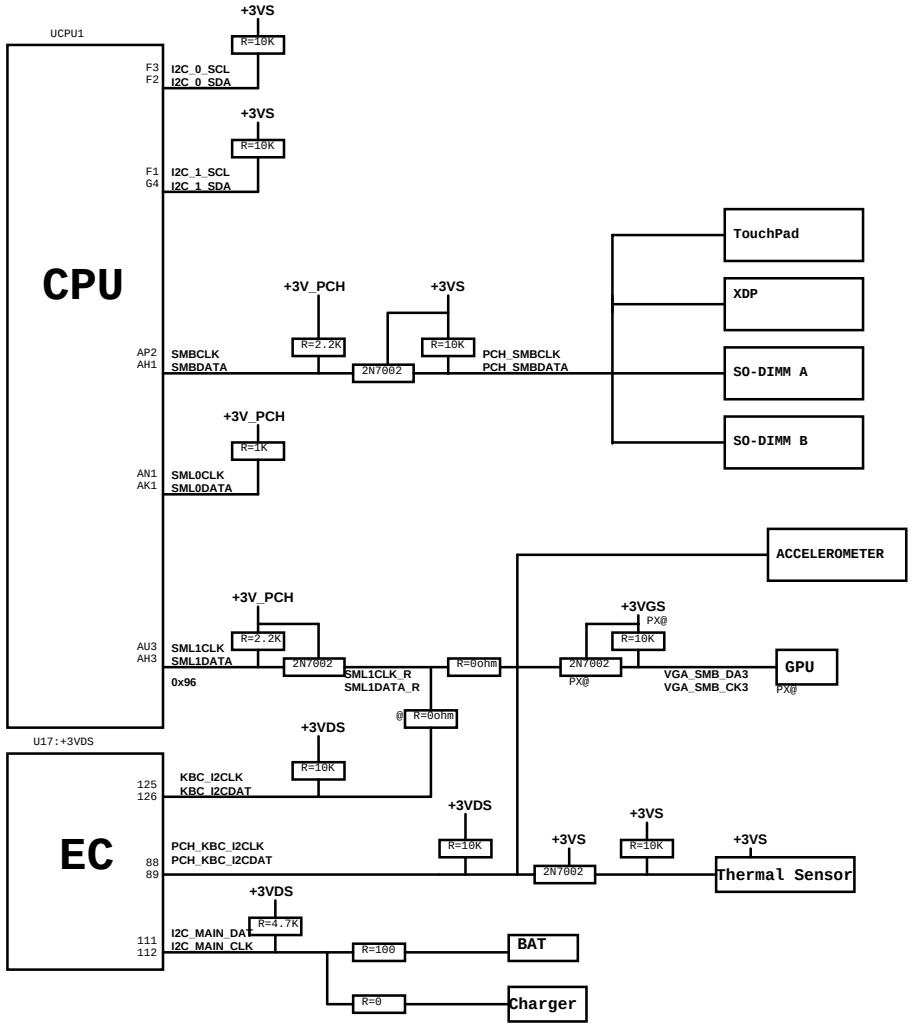
@ is NO SMT part (empty)
short@ : short pad , don't pop.
@EMI@,@ESD@,@RF@ : Reserve , don't pop.

RF@ : RF team request, must add.
EMI@ : EMI team request, must add.
ESD@ : ESD team request, must add.

LVDS@ : Support LVDS panel. **WWAN@ : For WWAN function.** **PX@ : GPU BOM config.**
eDP@ : Support eDP panel.



<USB2.0 port>

USB2.0 port	DESTINATION
	CS
0	USB 2.0(Right side)
1	USB 2.0(Right side)
2	USB 2.0(Left side)
3	WLAN/BT
4	Finger Print
5	WWAN (Option) Touch
6	Camera
7	USB 2.0(Left side)

<PCI-E,SATA,USB3.0>

Lane#	PCI-E		SATA	USB3.0	DESTINATION
					CS
1				0	USB3.0
2				1	USB3.0
3	1			2	WWAN (M.2)
4	2			3	Card reader(PCI-E)
5	3				10/100/1000 LAN
6	4				WLAN (M.2)
7	5				GPU(DIS only)
8					GPU(DIS only)
9					GPU(DIS only)
10					GPU(DIS only)
11	6	L3	3		2.5"HDD
12		L2	2		ODD
13		L1	1		
14		L0	0		SSD(NGFF)

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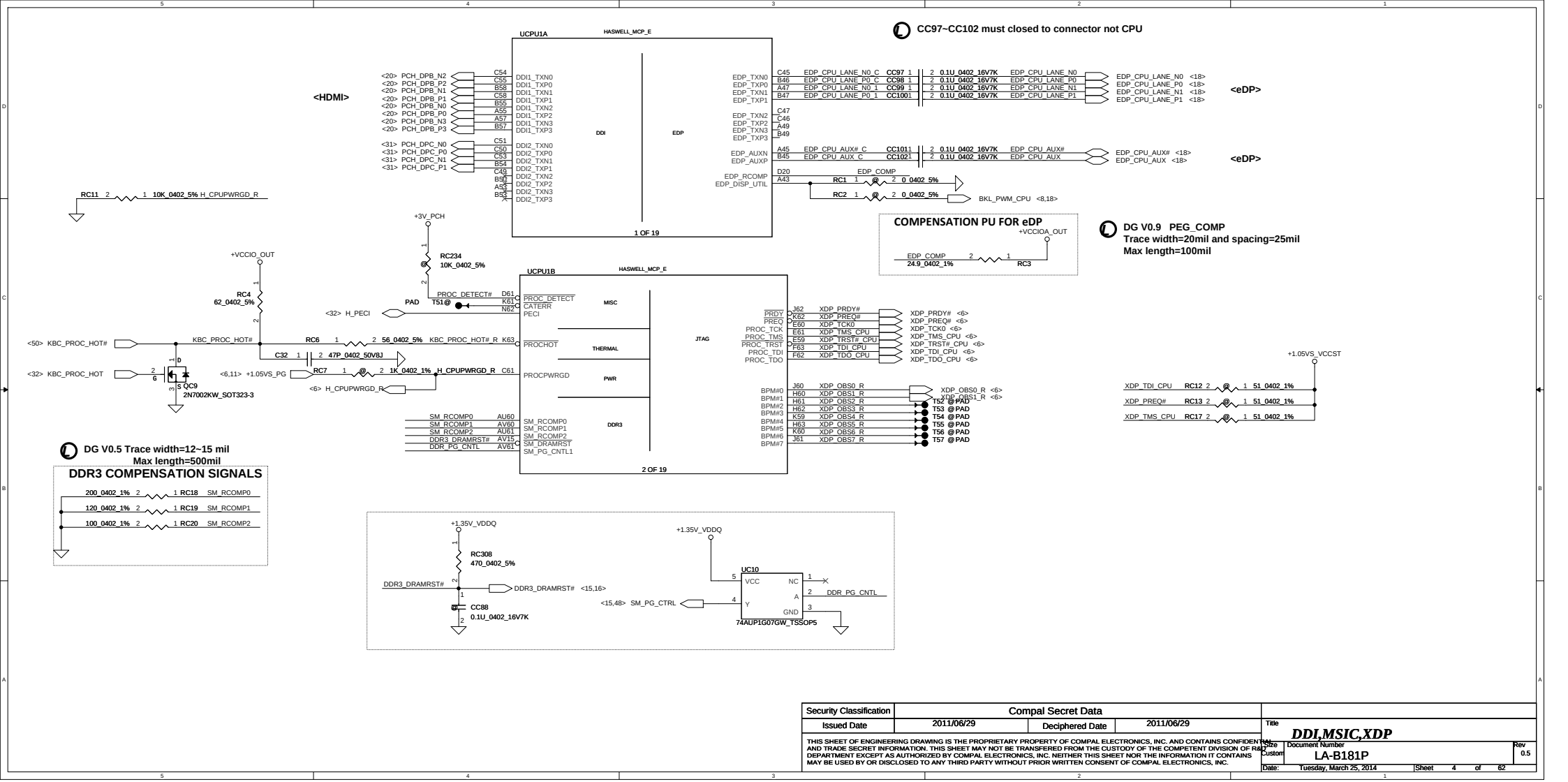

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Title: *DDI,MSIC,XDP*

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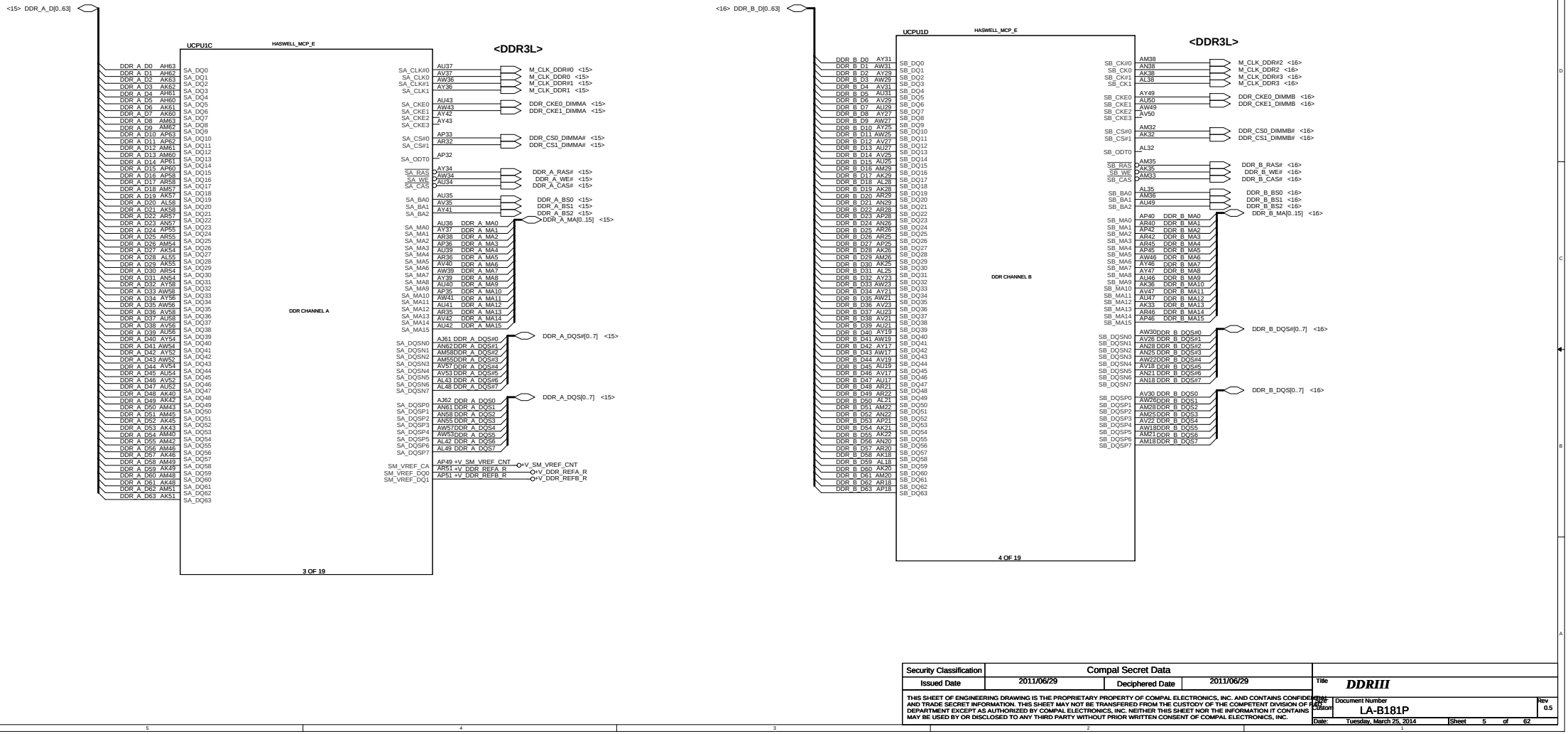

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INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable

+RTCVCC — 330K 0402 5% — RC236 PCH_INTVRMEN

+RTCVCC — CC2 1U_0402_6.3V6K — JCMOS1 SHORT PADS — CMOS
RC32 20K_0402_5% — PCH_RTCRST# — PCH_RTCRST# <8>
RC34 20K_0402_5% — PCH_SRTCRST#
CC5 1U_0402_6.3V6K — JME1 SHORT PADS — ME CMOS

PCH_RTCX1 — RC31 10M_0402_5% — PCH_RTCX2
YC1 32.768KHZ Q13FC1350000500
CC3 18P_0402_50V8J
CC4 18P_0402_50V8J

+RTCVCC — CC6 1U_0402_6.3V6K — 15mils — DC1 BAV70W 3P C/C_SOT-323 — 15mils — RC33 1K_0402_5% — +RTCBATT_R — +RTCBATT — JRTC1 LOTES_AAA-BAT-054-K01 CONN@
+3VDS

RTC BAT conn

+3VS
mSATA_DET# — RC219 43K_0402_5%
NMI_SMI_DBG# — RC327 10K_0402_5%
NMI_SMI_DBG# — @ESD@ C124 0.1U_0402_10V6K
mSATA_DET# — @RC225 10K_0402_5%

<32,44> BAT_GRNLED# — PLT_RST# — +3V_PCH
QC8A QC8B MESS84DW-G_SC88-6 MESS84DW-G_SC88-6
RC374 1K_0402_5% — HDA_SDOUT

+RTCVCC — RC36 1M_0402_5% — RC35 1M_0402_5%
<21> WWAN_DET# — Q89 2N7002KW_SOT323-3

HDA_SYNC_R — R11 short@ 0_0402_5% — HDA_SYNC

RP1
<26> HDA_BITCLK_AUDIO — HDA_BITCLK_AUDIO — HDA_BIT_CLK
<26> HDA_RST_AUDIO# — HDA_RST_AUDIO# — HDA_RST#
<26> HDA_SYNC_AUDIO — HDA_SYNC_R
<26> HDA_SDOUT_AUDIO — HDA_SDOUT_Q — HDA_SDOUT
33_0804_8P4R_5%
QC11 2N7002KW_SOT323-3

CM28 — HDA_BITCLK_AUDIO — 22P_0402_50V8J
CM29 — HDA_RST_AUDIO# — 22P_0402_50V8J

11/28 — +5VS — RC222 10K_0402_5%

PAD T156
PAD T157

UCPU1E — HASWELL_MCP_E

PCH_RTCX1	AW5	RTCX1
PCH_RTCX2	AY5	RTCX2
SM_INTRUDER#	AU6	INTRUDER
PCH_INTVRMEN	AV7	INTVRMEN
PCH_SRTCRST#	AV6	SRTCRST
PCH_RTCRST#	AU7	RTCRST
		RTC
HDA_BIT_CLK	AW8	HDA_BCLK/I2S0_SCLK
HDA_SYNC	AV11	HDA_SYNC/I2S0_SFRM
HDA_RST#	AU8	HDA_RST/I2S_MCLK
HDA_SDI0	AY10	HDA_SDI0/I2S0_RXD
HDA_SDOUT	AU12	HDA_SDI1/I2S1_RXD
	AU11	HDA_SDO/I2S0_TXD
	AW10	DOCKEN/I2S1_TXD
	AV10	HDA_DOCK_RST/I2S1_SFRM
	AY8	I2S1_SCLK
		AUDIO
PCH_JTAG_RST#	AU62	PCH_TRST
PCH_JTAG_TCK	AE62	PCH_TCK
PCH_JTAG_TDI	AD61	PCH_TDI
PCH_JTAG_TDO	AE61	PCH_TDO
PCH_JTAG_TMS	AD62	PCH_TMS
	AL11	TP5
	AC4	TP6
XDP_TCK_JTAGX	AE63	JTAGX
	AV2	RSVD
		JTAG

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SATA_RN0/PERN6_L3 — J5 — SATA_PRX_DTX_N0 <22>
SATA_RP0/PERP6_L3 — H5 — SATA_PRX_DTX_P0 <22>
SATA_TN0/PETN6_L3 — B15 — SATA_PTX_DRX_N0 <22>
SATA_TP0/PETP6_L3 — A15 — SATA_PTX_DRX_P0 <22>
2.5" SSD/HDD

SATA_RN1/PERN6_L2 — J8 — SATA_PRX_DTX_N1 <22>
SATA_RP1/PERP6_L2 — H8 — SATA_PRX_DTX_P1 <22>
SATA_TN1/PETN6_L2 — A17 — SATA_PTX_DRX_N1 <22>
SATA_TP1/PETP6_L2 — B17 — SATA_PTX_DRX_P1 <22>
ODD

SATA_RN2/PERN6_L1 — J6 — SATA_PRX_DTX_N2 <21>
SATA_RP2/PERP6_L1 — H6 — SATA_PRX_DTX_P2 <21>
SATA_TN2/PETN6_L1 — B14 — SATA_PTX_DRX_N2 <21>
SATA_TP2/PETP6_L1 — C15 — SATA_PTX_DRX_P2 <21>
WWAN (M.2 slot)

SATA_RN3/PERN6_L0 — F5 — SATA_PRX_DTX_N3 <21>
SATA_RP3/PERP6_L0 — E5 — SATA_PRX_DTX_P3 <21>
SATA_TN3/PETN6_L0 — C17 — SATA_PTX_DRX_N3 <21>
SATA_TP3/PETP6_L0 — D17 — SATA_PTX_DRX_P3 <21>

SATA0GP/GPIO34 — V1 — AMD_VBIOS_SEL0
SATA1GP/GPIO35 — U1 — AMD_VBIOS_SEL1
SATA2GP/GPIO36 — V6 — NMI_SMI_DBG# — NMI_SMI_DBG# <32>
SATA3GP/GPIO37 — AC1 — mSATA_DET# — mSATA_DET# <21>

SATA_IREF — A12 — RC39 3K_0402_1% — +1.05VS_VCCSATA3PLL
TP7 — L11
TP8 — K10
SATA_RCOMP — C12 — SATA_COMP
SATALED — U3 — SATA_ACT# — SATA_ACT# <7,43>

<Page 12>
DG V0.9 SATA_COMP
Width=12mil
Max length=500mil

VBIOS ID TALBE

+3VS — RC218 10K_0402_5% — UMA@ — AMD_VBIOS_SEL0
10/24 Add VBIOS select
PX@ RC220 100K_0402_5%

GPIO35 (SEL1)	GPIO34 (SEL0)	
0	0	VBIOS1
0	1	VBIOS2
1	0	VBIOS3
1	1	UMA

11/28
+3VS — RC217 10K_0402_5% — UMA@ — AMD_VBIOS_SEL1
PX@ RC221 100K_0402_5%

+1.05VS_VCCST
12/28
RC283 51_0402_1% — PCH_JTAG_TDO
RC41 @ 51_0402_1% — PCH_JTAG_TDI
RC45 @ 51_0402_1% — PCH_JTAG_TMS
RC46 @ 51_0402_1% — XDP_TCK_JTAGX

<CPU site>

PWR_GD — RC240 @ 10K_0402_5% — +3VS — @CC86 .1U_0402_16V7K

XDP@ UC5 74CBTLV3126DS_SSOP16

	1OE	VCC	16
XDP_TDO_CPU	1A	1B	XDP_TDO
	2OE		
XDP_TDI_CPU	2A	2B	XDP_TDI_SWITCH
	3OE		
XDP_TMS_CPU	3A	3B	XDP_TMS
	4OE		
XDP_TRST#_CPU	4A	4B	XDP_TRST#
		NC	1
	GND	NC	9

+VCCIO_OUT — CC125 .01U_0402_16V4Z — CC126 2.2U_0402_6.3V6M
Place near JXDP1

+VCCIO_OUT — +VCCIO_OUT

JXDP1 SAMTE_BSH-030-01-L-D-A CONN@

	GND0	GND1	
<4> XDP_PREQ#	XDP_PREQ#	OBSFN_C0	CFG17 <14>
<4> XDP_PRDY#	XDP_PRDY#	OBSFN_C1	CFG16 <14>
	OBSFN_A0	GND3	
<14> CFG0	CFG0	OBSDATA_C0	CFG8 <14>
<14> CFG1	CFG1	OBSDATA_C1	CFG9 <14>
	OBSDATA_A0	GND5	
<14> CFG2	CFG2	OBSDATA_C2	CFG10 <14>
<14> CFG3	CFG3	OBSDATA_C3	CFG11 <14>
	OBSDATA_A1	GND7	
	OBSDATA_A2	OBSFN_D0	CFG19 <14>
<4> XDP_OBS0_R	XDP_OBS0_R	OBSFN_D1	CFG18 <14>
<4> XDP_OBS1_R	XDP_OBS1_R	GND9	
	OBSDATA_A3	OBSDATA_D0	CFG12 <14>
<14> CFG4	CFG4	OBSDATA_D1	CFG13 <14>
<14> CFG5	CFG5	GND11	
	OBSDATA_B0	OBSDATA_D2	CFG14 <14>
<14> CFG6	CFG6	OBSDATA_D3	CFG15 <14>
<14> CFG7	CFG7	GND13	
	OBSDATA_B1	ITPCLK/HOOK4	CLK_CPU_ITP <7>
	GND10	ITPCLK#/HOOK5	CLK_CPU_ITP# <7>
	OBSDATA_B2	VCC_OBS_CD	
	OBSDATA_B3	RESET#/HOOK6	XDP_RST# R RC373 2 1K_0402_1% — PLT_RST# <8,21,23,30,32,33,43>
	GND12	DBR#/HOOK7	XDP_DBRESET# — XDP_DBRESET# <8>
	PWRGOOD/HOOK0	GND15	
	HOOK1	TDO	XDP_TDO
	VCC_OBS_AB	TRST#	XDP_TRST#
	HOOK2	TDI	XDP_TDI
	HOOK3	TMS	XDP_TMS
	GND14	GND17	RC372 2 1 CFG3 1K_0402_1%
	SDA		
	SCL		
	TCK1		
	TCK0		
	GND16		

RC17 need to close to JCPU1
H_CPUPWRGD_R — RC371 1 2 1K_0402_1% — H_CPUPWRGD_XDP
<4> H_CPUPWRGD_R
<8,32> ON/OFFBTN#
<11> CPU_PWR_DEBUG
<8,32> PM_PWROK
<7,15,16,43> PCH_SMBDATA
<7,15,16,43> PCH_SMBCLK
XDP_TCK1
XDP_TCK0

<XDP> — XDP_TRST# CPU — RC37 0_0402_5% — PCH_JTAG_RST# — <PCH site>
<XDP> — XDP_TMS — RC201 short@ 0_0402_5% — PCH_JTAG_TMS — <PCH site>
<CPU>
<PCH site> — PCH_JTAG_TDO — RC307 @ 0_0402_5% — XDP_TDI — <XDP>
<XDP> — XDP_TDI — RC200 short@ 0_0402_5% — XDP_TDI_SWITCH — <EC output>
<PCH site> — PCH_JTAG_TDI — RC195 short@ 0_0402_5% — XDP_TDI — <XDP>
<XDP> — XDP_TDO — RC194 short@ 0_0402_5% — PCH_JTAG_TDO — <PCH site>

+1.05VS_VCCST — +3V_PCH — R511 10K_0402_5%
U16 74AUP1G07GW_TSSOP5
<8,32,41> PWR_GD — PWR_GD — +1.05VS_PG <4,11>

<CPU,XDP,XDP Switch>

XDP_TCK:XDP contact with CPU No 0ohm(RS5)

PCH_JTAG_TCK — RC38 @ 51_0402_5%
XDP_TRST# CPU — RC16 @ 51_0402_1%
XDP_TCK0 — RC15 @ 51_0402_1%

<PCH site> — PCH_JTAG_TCK — RC196 short@ 0_0402_5% — XDP_TCK1
<PCH site> — PCH_JTAG_TCK — RC197 @ 0_0402_5% — XDP_TCK0 — XDP_TCK0 <4> — <CPU and XDP>
<PCH site> — XDP_TCK_JTAGX — RC193 short@ 0_0402_5%
<PCH site> — XDP_TCK_JTAGX — RC306 @ 0_0402_5% — XDP_TDO — <XDP>

+1.05VS_VCCST — XDP_TDO_CPU — RC10 @ 51_0402_1%
+1.05VS_VCCST — XDP_TDO — RC14 @ 51_0402_1%

Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3d**,J4d, R6,R7,R8,R9

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Title: RTC,SATA,HDA,JTAG
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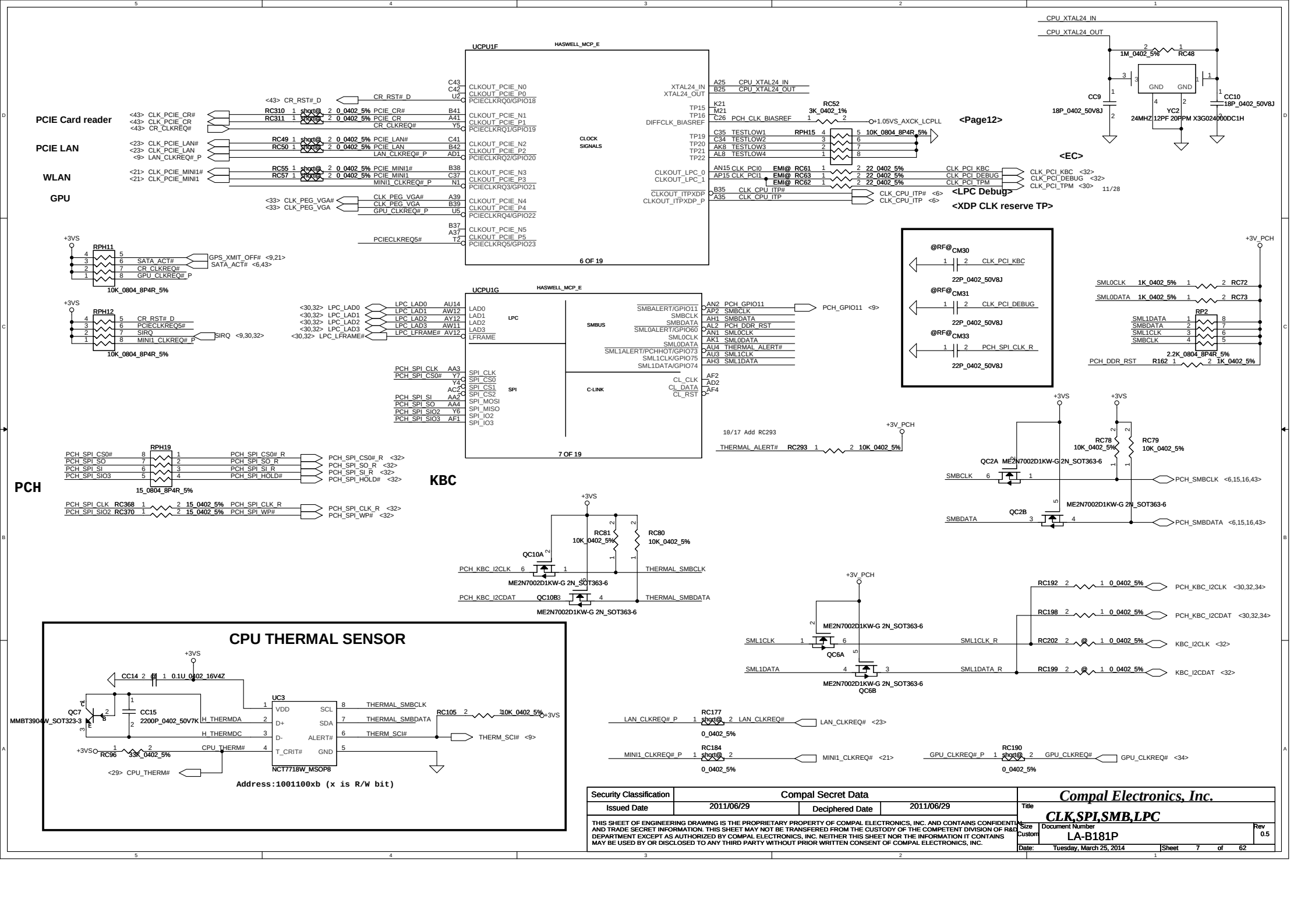
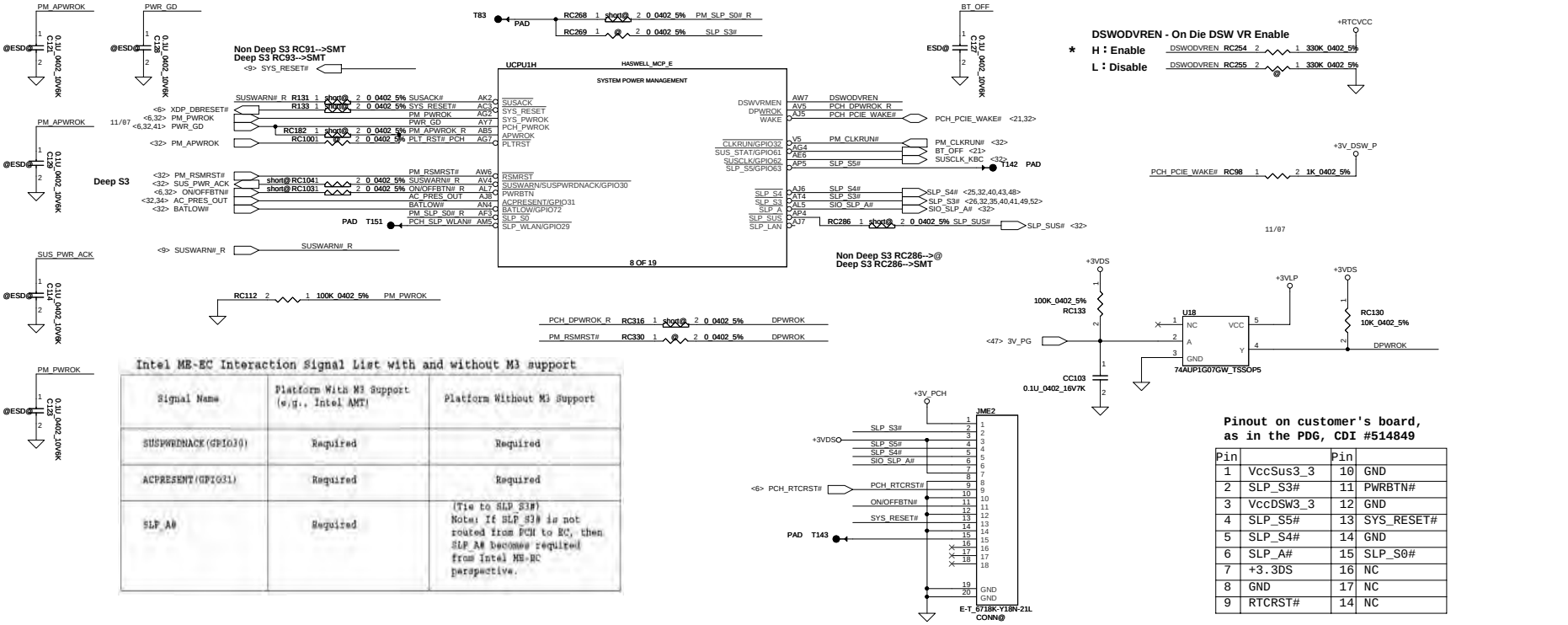
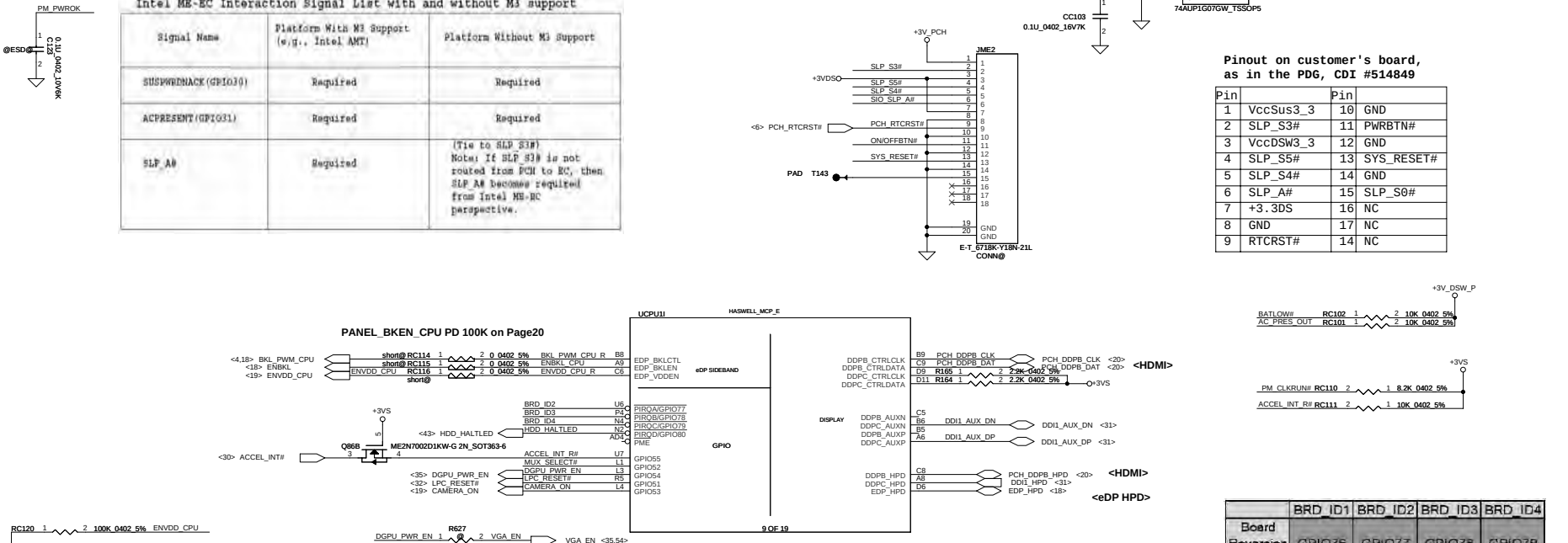

PCIE Card reader
PCIE LAN
WLAN
GPU
PCH
KBC
UCPU1F
HASWELL_MCP_E
CLOCK SIGNALS
6 OF 19
UCPU1G
LPC
SMBUS
C-LINK
SPI
7 OF 19
<Page12>
<EC>
<LPC Debug>
<XDP CLK reserve TP>
CPU THERMAL SENSOR
UC3
NCT7718W_MSOP8
Address:1001100xb (x is R/W bit)
Compal Secret Data
Compal Electronics, Inc.
CLK,SPI,SMB,LPC
LA-B181P
Tuesday, March 25, 2014



Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC perspective.

Pin		Pin	
1	VccSus3_3	10	GND
2	SLP_S3#	11	PWRBTN#
3	VccDSW3_3	12	GND
4	SLP_S5#	13	SYS_RESET#
5	SLP_S4#	14	GND
6	SLP_A#	15	SLP_S0#
7	+3.3DS	16	NC
8	GND	17	NC
9	RTCRST#	14	NC



Board Reversion	BRD_ID1 GPIO76	BRD_ID2 GPIO77	BRD_ID3 GPIO78	BRD_ID4 GPIO79
0.1 DB0	0	0	0	0
DB1	0	0	0	1
0.2 DB2	0	0	1	0
0.3	0	0	1	1
0.4 SI1	0	1	0	0
SI1B	0	1	0	1
SI2	0	1	1	0
	0	1	1	1
0.5 PV1	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
MV	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

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Title: PM,GPIO,DDI

Size: Custom | Document Number: LA-B181P | Rev: 0.5

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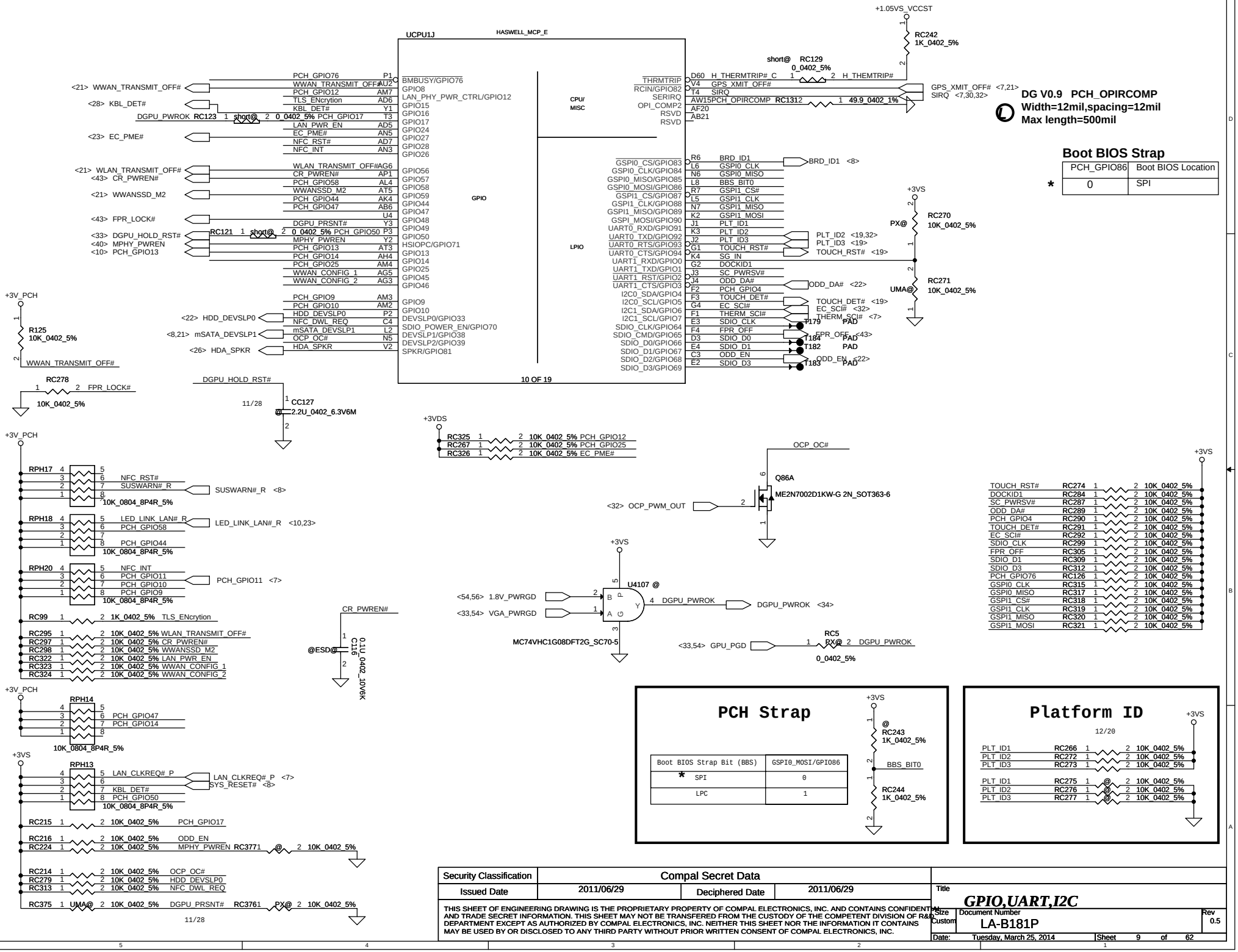

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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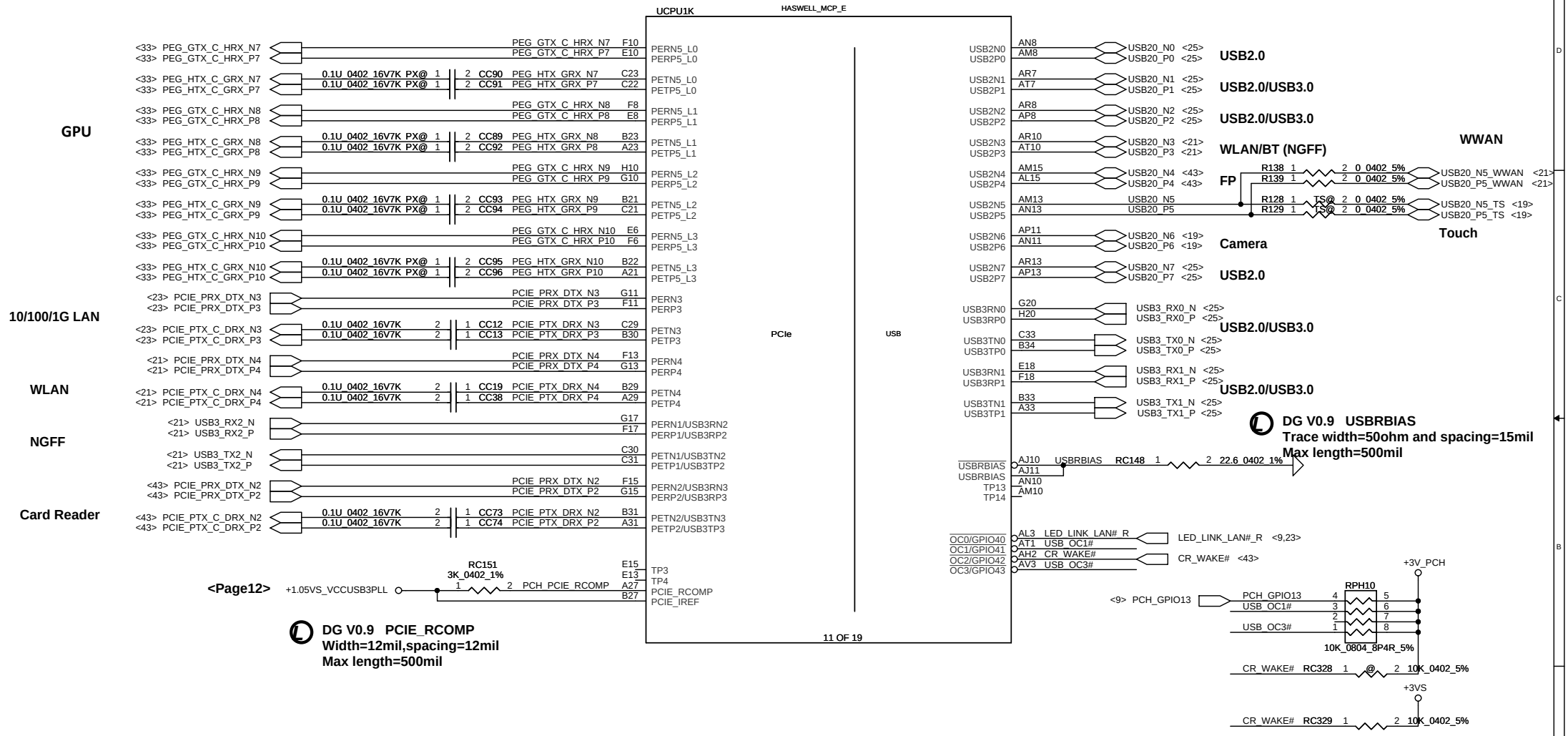
Title	GPIO,UART,I2C		
Size	Document Number		Rev
Custom	LA-B181P		0.5
Date:	Tuesday, March 25, 2014	Sheet	9 of 62



Security Classification	Compal Secret Data			
Issued Date	2011/06/29	Deciphered Date	2011/06/29	

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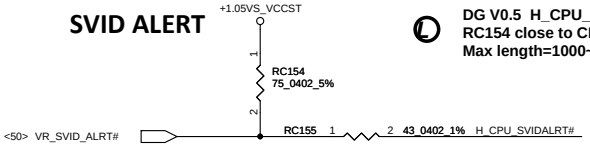
Title	PCIE,USB		
Size	Document Number		Rev
B	LA-B181P		0.5
Date: Tuesday, March 25, 2014	Sheet 10 of 62		

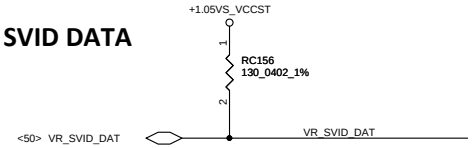
+VCC_CORE@10000mA

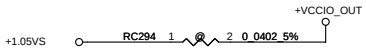
SVID ALERT



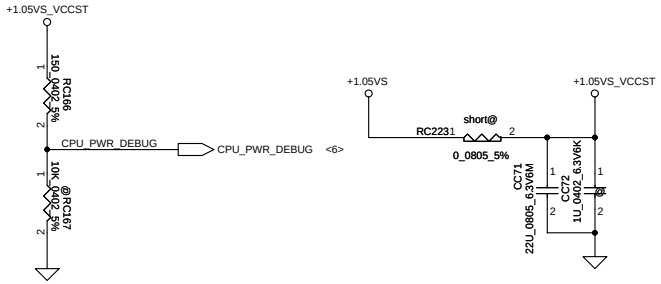
DG V0.5 H_CPU_SVIDALRT#
RC154 close to CPU<300mil
Max length=1000~2000mil

SVID DATA

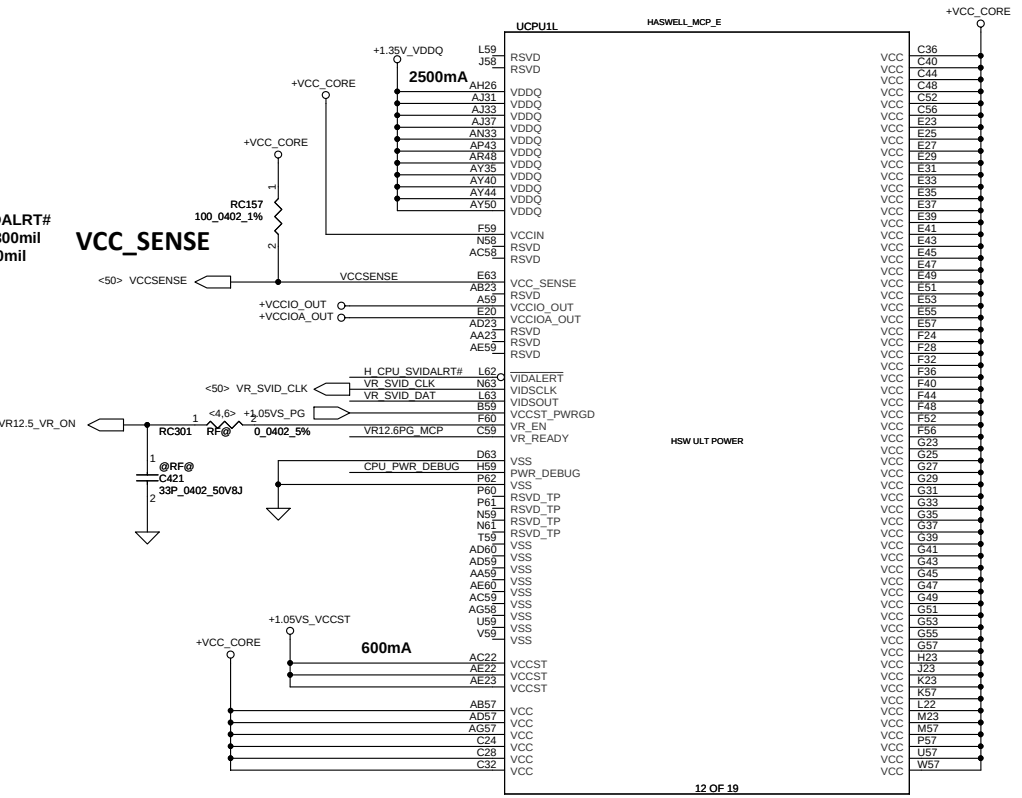


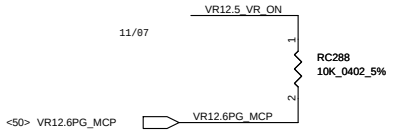


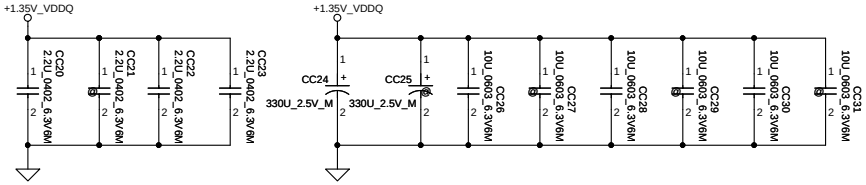
DG V0.5 VIDSOUT
RC156 close to CPU<500mil
Max length=1000~2000mil



VCC_SENSE







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Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Compal Electronics, Inc.

Title: Power

Size	Document Number	Rev
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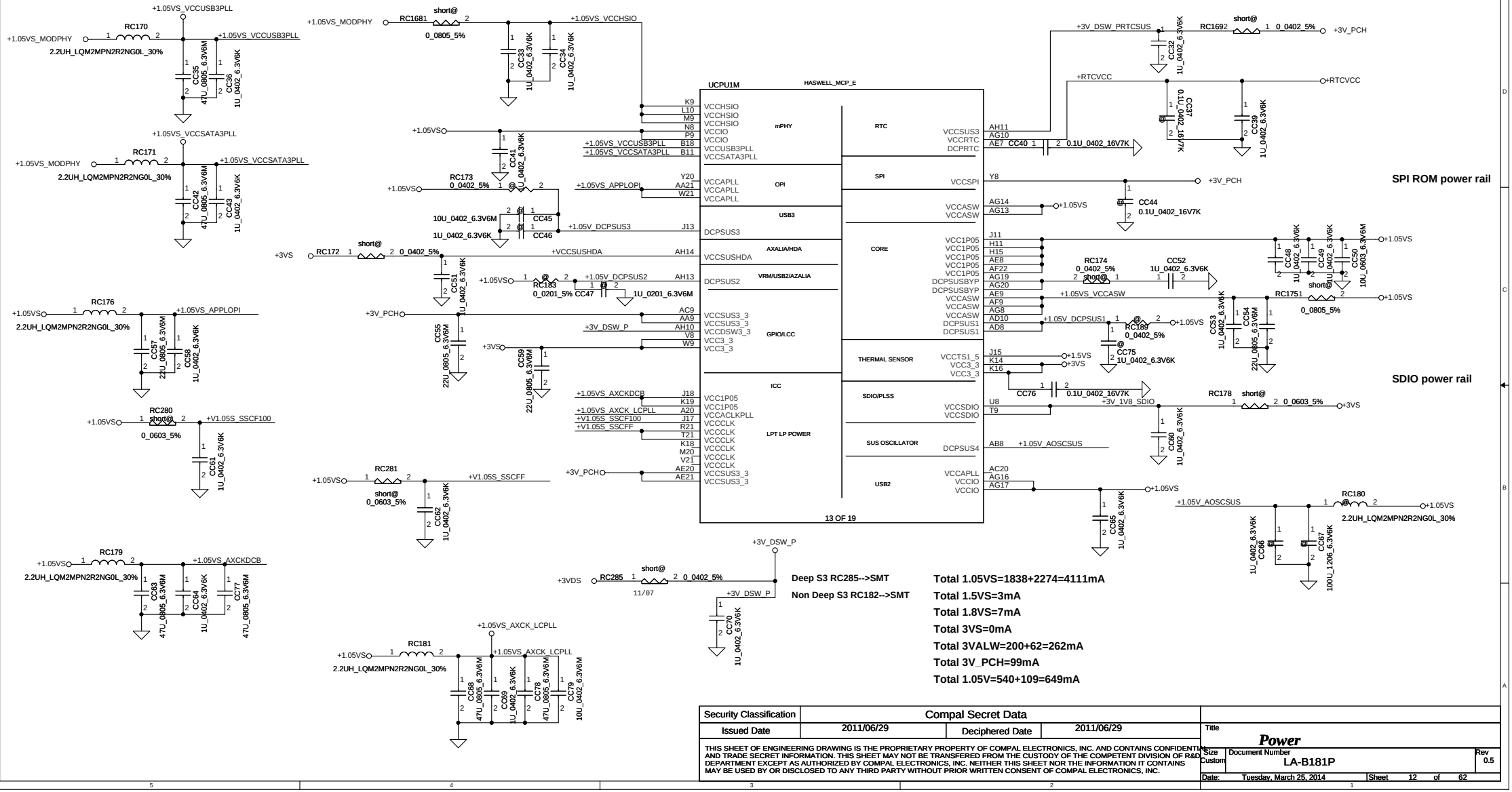

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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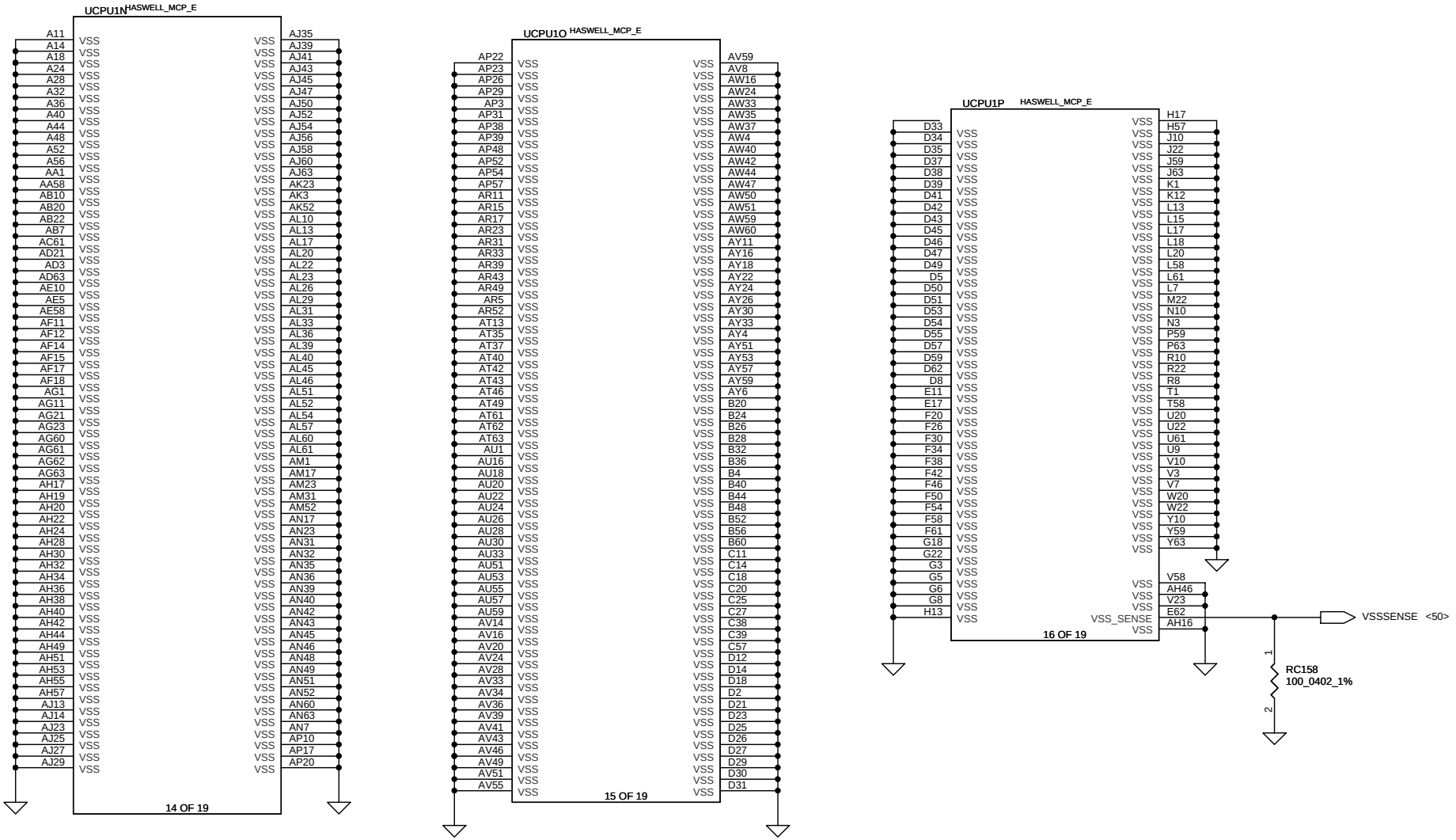
Title	Power		
Size: Custom	Document Number: LA-B181P		Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 12 of 62		



Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

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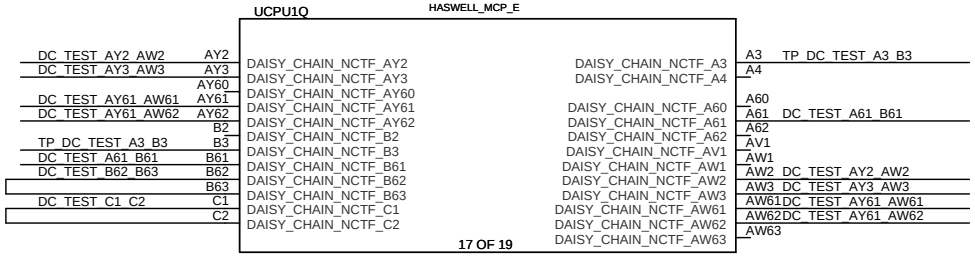
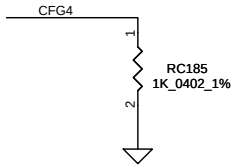
Compal Electronics, Inc.

Title: GND/VSSSEN

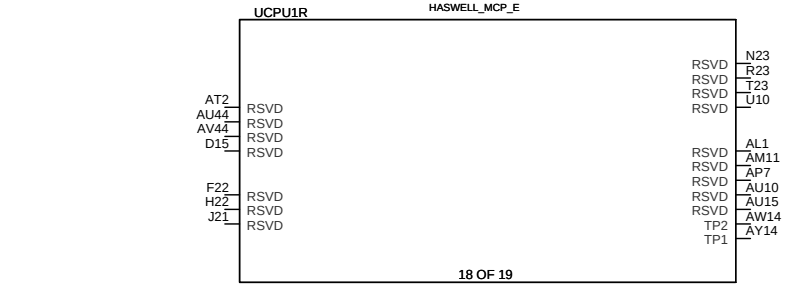
Size | Document Number: LA-B181P | Rev: 0.5

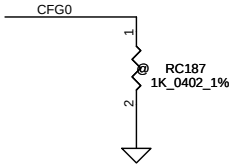
Date: Tuesday, March 25, 2014 | Sheet 13 of 62

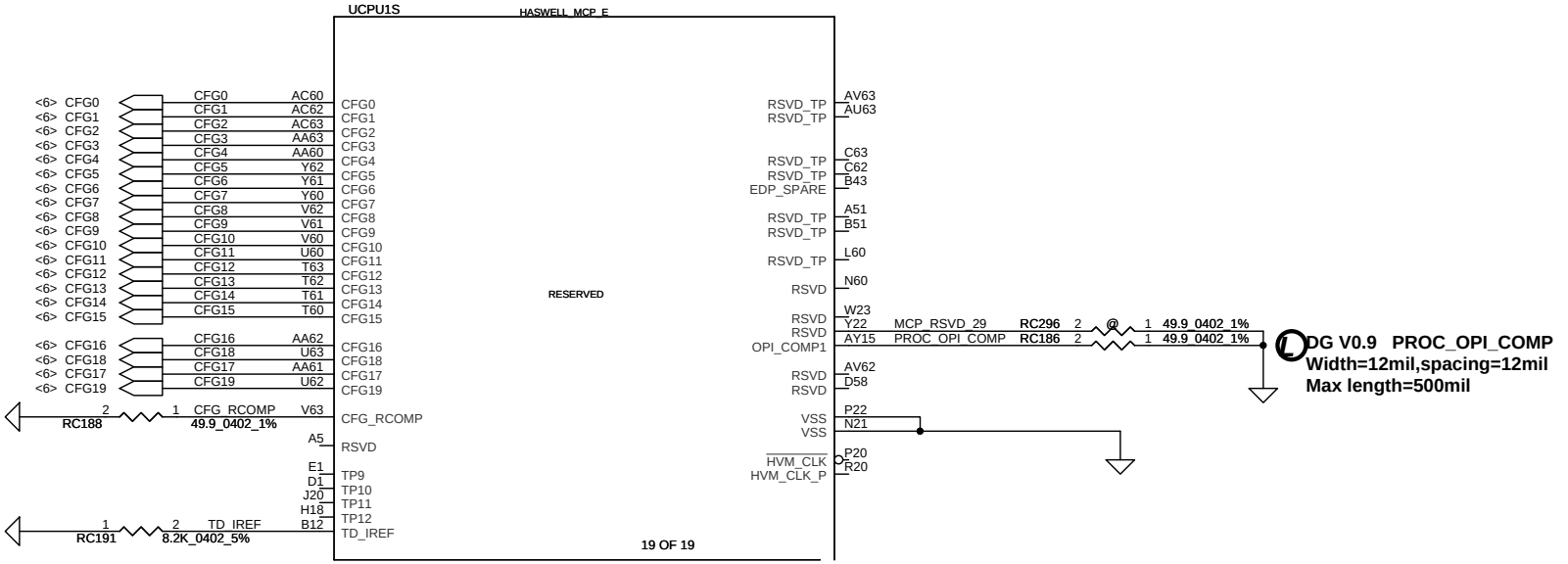




Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port







Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Compal Electronics, Inc.

Title: **RSVD/CFG**

Size	Document Number	Rev
	LA-B181P	0.5

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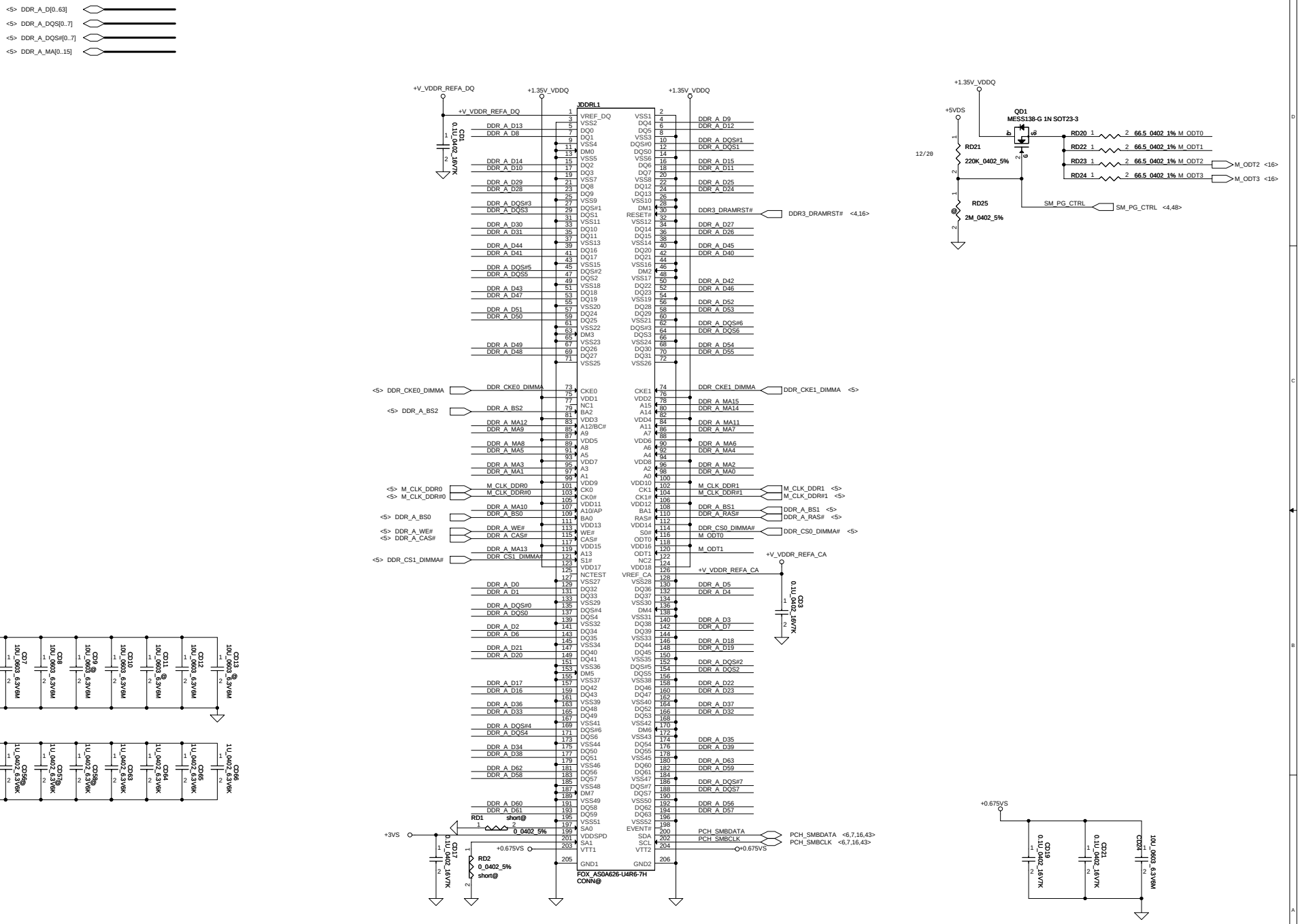

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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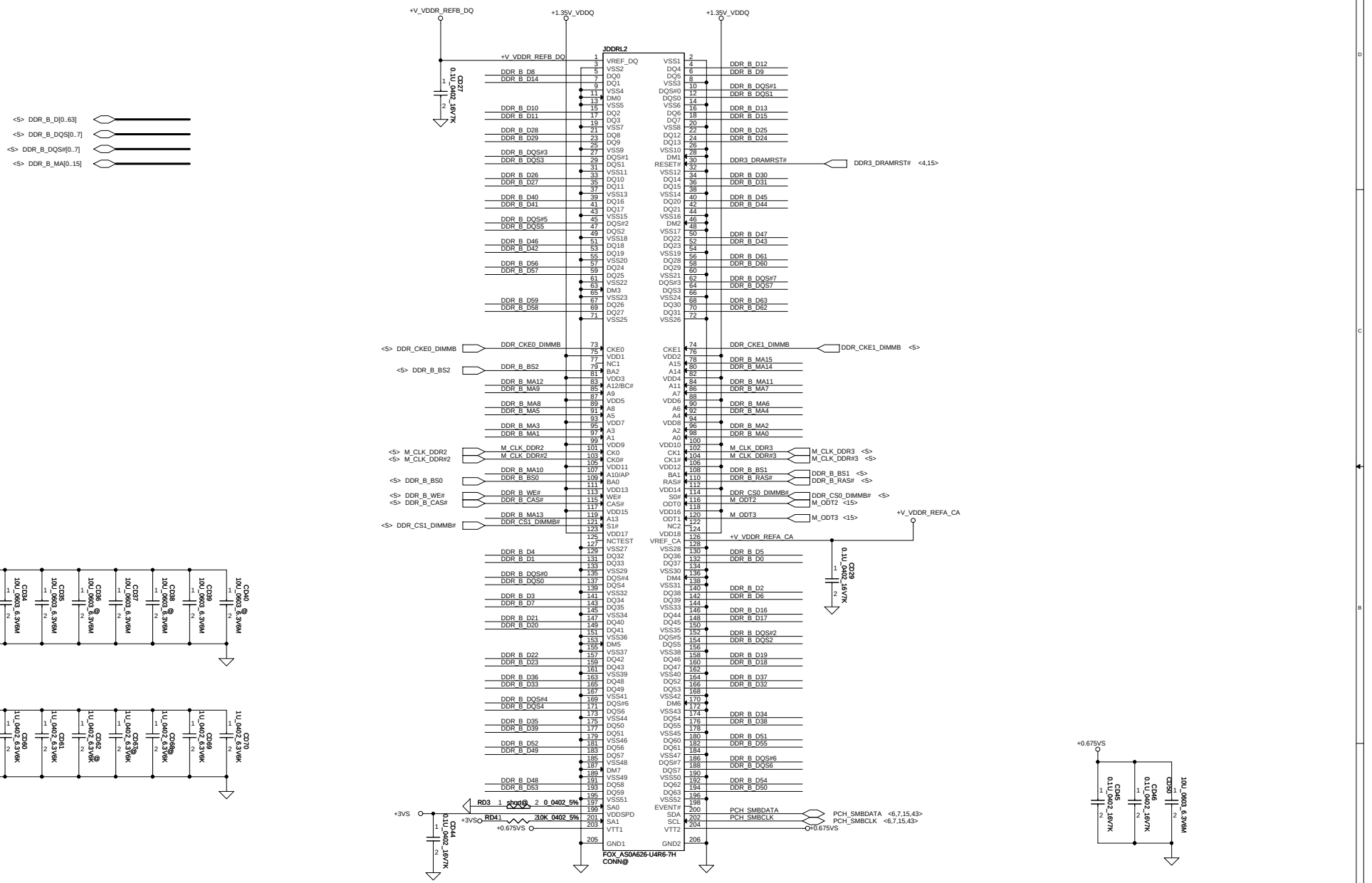
Title: ***DDR3L DIMM0***

Size	Document Number	Rev
C	LA-B181P	0.5

Date: Tuesday, March 25, 2014 | Sheet 15 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

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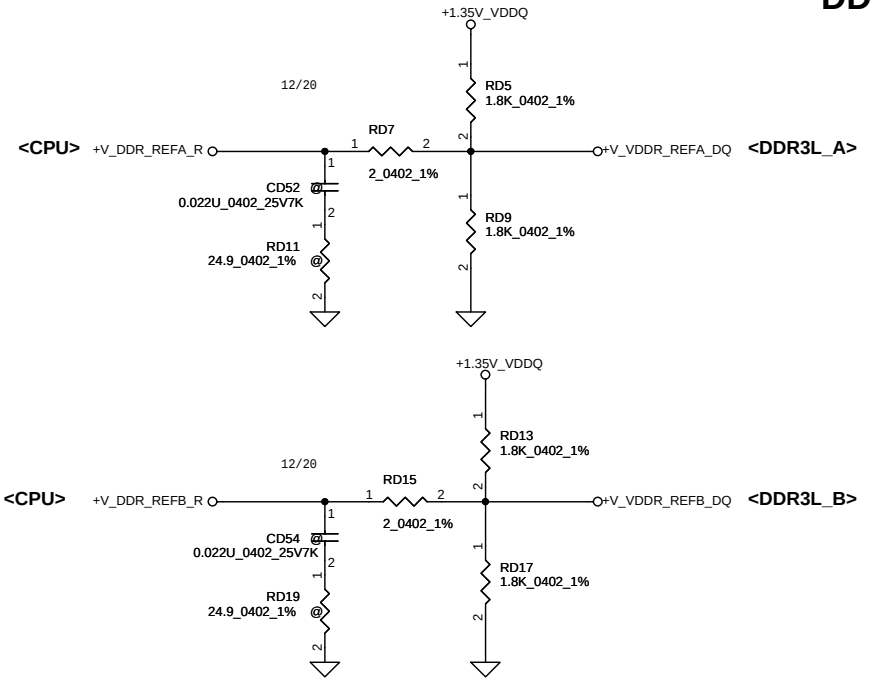
Compal Electronics, Inc.

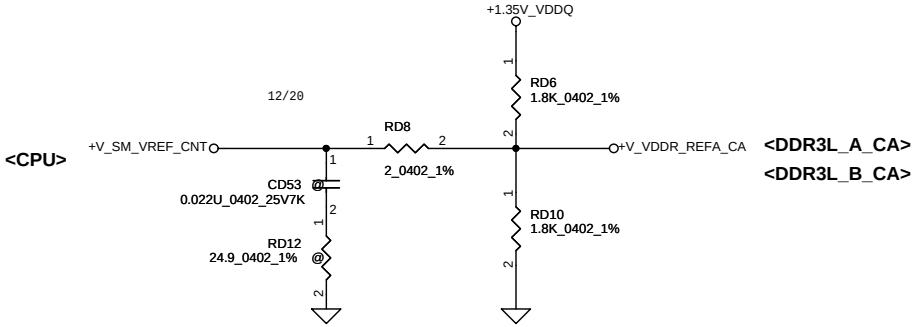
Title: DDR3L DIMM1

Size	Document Number	Rev
	LA-B181P	0.5

Date: Tuesday, March 25, 2014 | Sheet 16 of 62

DDR3L VREF





Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Compal Electronics, Inc.

Title: DDR3L VREF

Size: | Document Number: LA-B181P | Rev: 0.5

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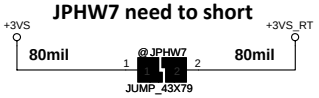
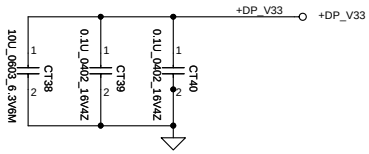
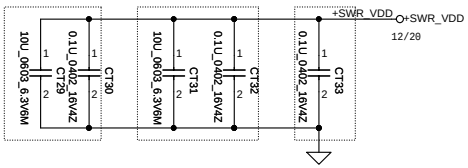
JPHW7 need to short



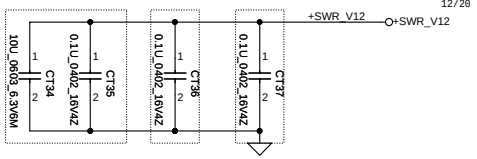
Layout note
Close to Pin3



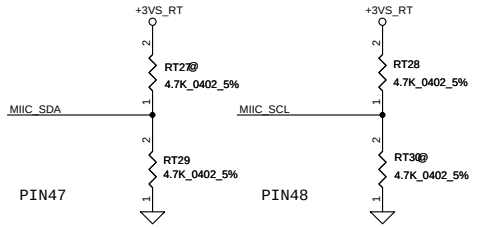
Layout note
Close to LT5 Close to Pin18 Close to Pin13



Layout note
Close to Pin11 Close to Pin27 Close to Pin7



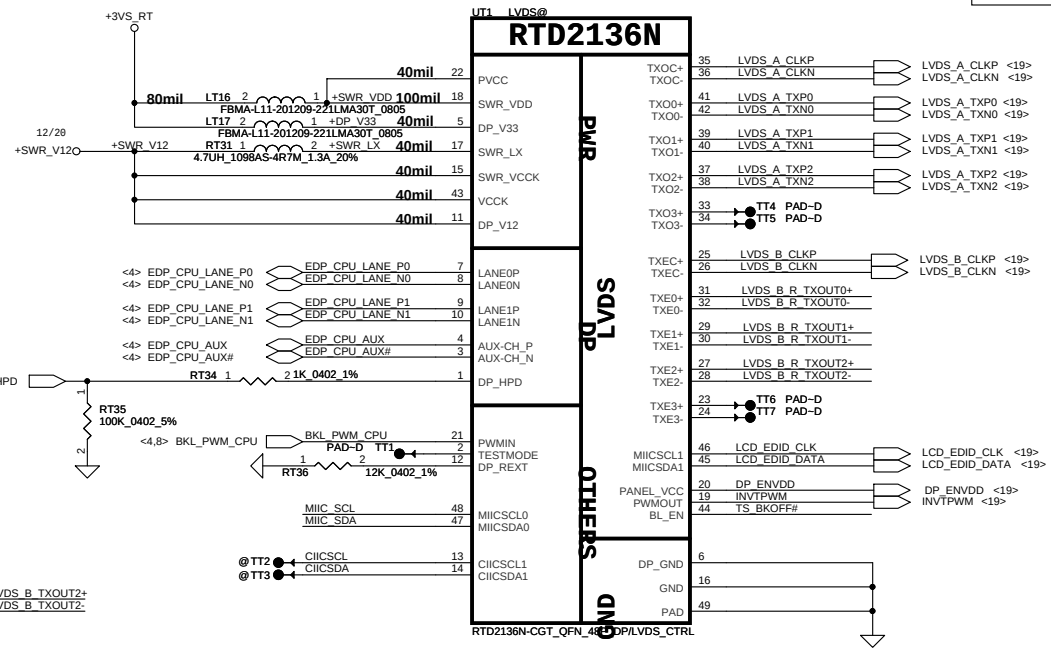
※ROM only mode : PIN 47 4.7k pull low, Pin 48 4.7k pull high.
EP mode : PIN 47 4.7k pull high, Pin 48 4.7k pull low.
EEPROM : PIN 47 4.7k pull high, Pin 48 4.7k pull high.
〈 ※Default mode 〉

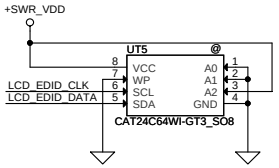


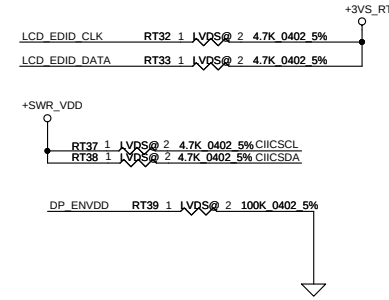
SWR / LDO Mode select

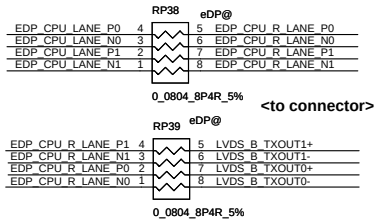
	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

※ If use 2132R, please select LDO mode as default.









<to connector>

EDP_CPU_AUX RT43 eDP@ 0_0402_5% EDP_CPU_R_AUX RT45 eDP@ 0_0402_5% LVDS_B_TXOUT2+
EDP_CPU_AUX# RT44 eDP@ 0_0402_5% EDP_CPU_R_AUX# RT46 eDP@ 0_0402_5% LVDS_B_TXOUT2-

LVDS_B_R_TXOUT1+ RT53 LVDS@ 0_0402_5% LVDS_B_TXOUT1+ → LVDS_B_TXOUT1+ <19>
LVDS_B_R_TXOUT1- RT54 LVDS@ 0_0402_5% LVDS_B_TXOUT1- → LVDS_B_TXOUT1- <19>
LVDS_B_R_TXOUT0+ RT55 LVDS@ 0_0402_5% LVDS_B_TXOUT0+ → LVDS_B_TXOUT0+ <19>
LVDS_B_R_TXOUT0- RT56 LVDS@ 0_0402_5% LVDS_B_TXOUT0- → LVDS_B_TXOUT0- <19>

LVDS_B_R_TXOUT2+ RT47 LVDS@ 0_0402_5% LVDS_B_TXOUT2+ → LVDS_B_TXOUT2+ <19>
LVDS_B_R_TXOUT2- RT48 LVDS@ 0_0402_5% LVDS_B_TXOUT2- → LVDS_B_TXOUT2- <19>

EDP_HPD RT49 eDP@ 0_0402_5% EDP_HPD_PANEL RT51 eDP@ 0_0402_5% EDP_HPD_PANEL_R → EDP_HPD_PANEL_R <19>
BKL_PWM_CPU RT50 eDP@ 0_0402_5% INVTPWM

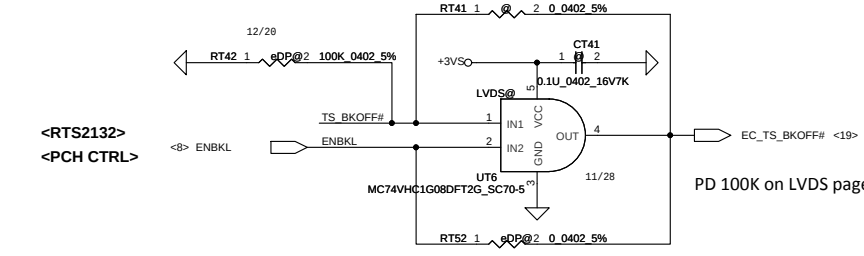
<LVDS panel>

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform



<RTS2132>
<PCH CTRL>

PD 100K on LVDS page

<LVDS Panel>

Different between 2132S and 2132R	
2132S	**2132R**
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

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Compal Electronics, Inc.

Title: *LVDS Translator-RTD2132R*

Size: | Document Number: LA-B181P | Rev: 0.5

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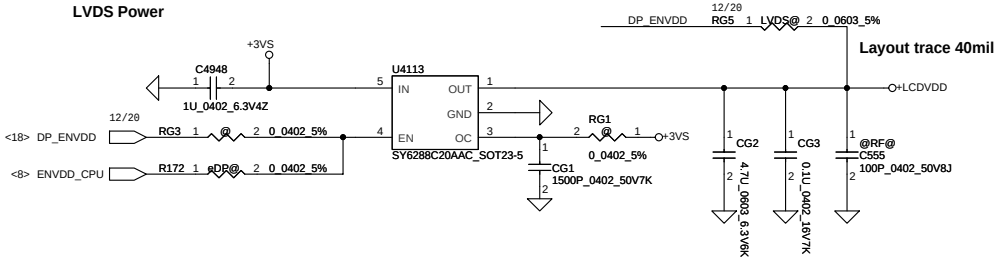
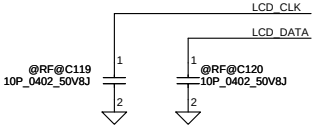
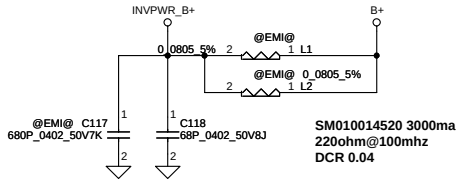
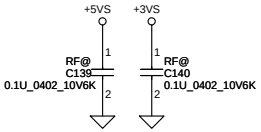
LVDS Power



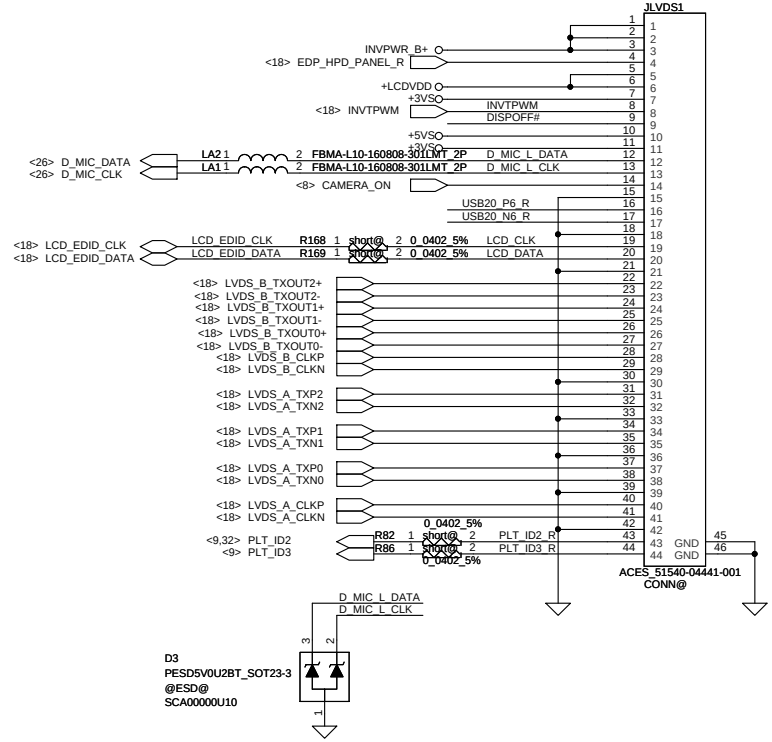


W=60mils W=60mils





LCD/LED PANEL Conn.



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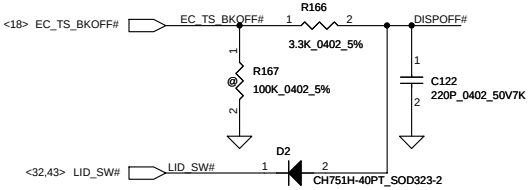

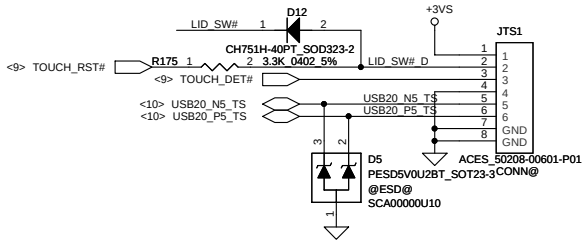

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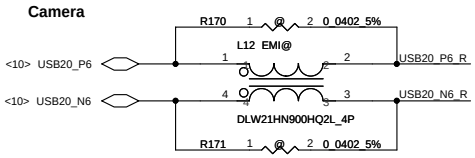

	GPIO92 PLT_ID2	GPIO93 PLT_ID3
Rolo 14"	0	1
Reeses 15"	1	0
Raisinet 17"	1	1

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: **LVDS Connector**

Size	Document Number	Rev
	LA-B181P	0.5

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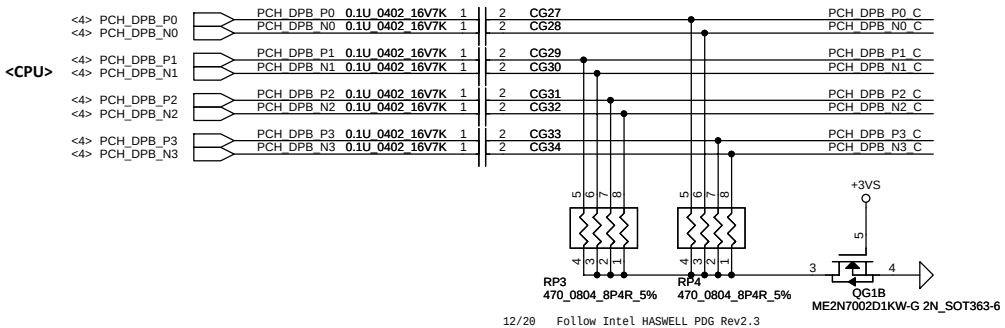
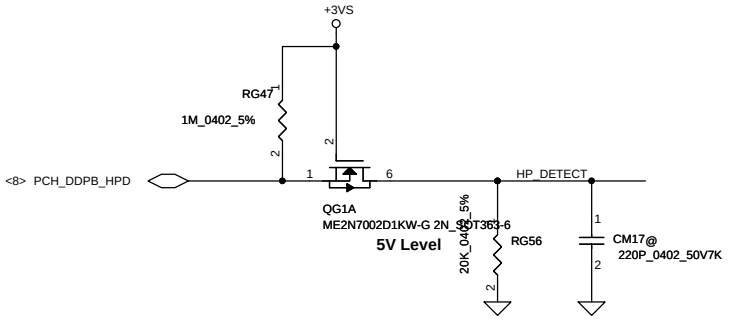
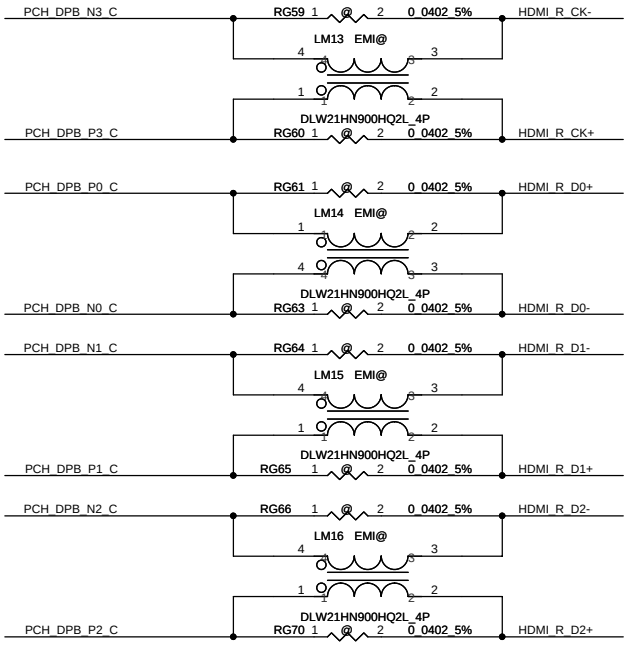
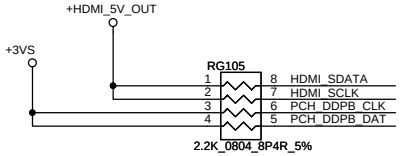
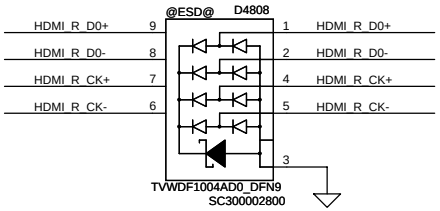


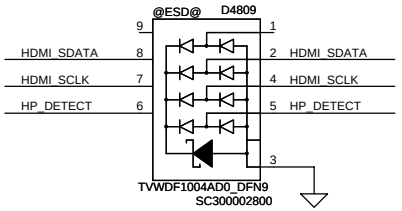
12/20 Follow Intel HASWELL PDG Rev2.3

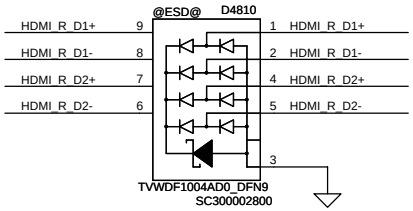


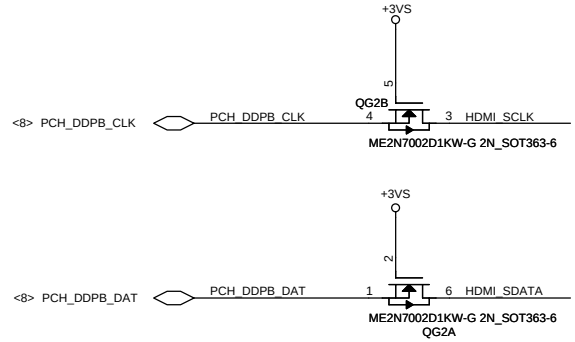






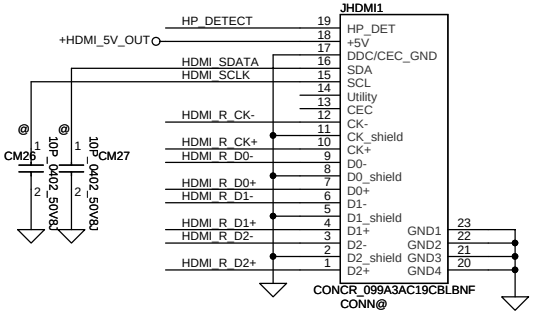




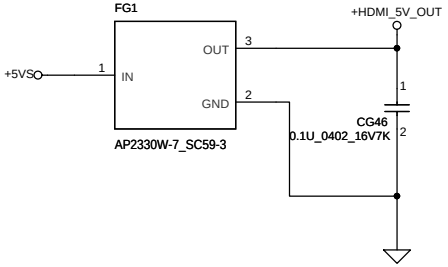


5V PULL UP IN CONNECTER SIDE

HDMI Conn.



W=40mils



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Compal Electronics, Inc.	
Title	HDMI Conn/Level shift
Size	Document Number: LA-B181P
Rev	0.5
Date:	Tuesday, March 25, 2014
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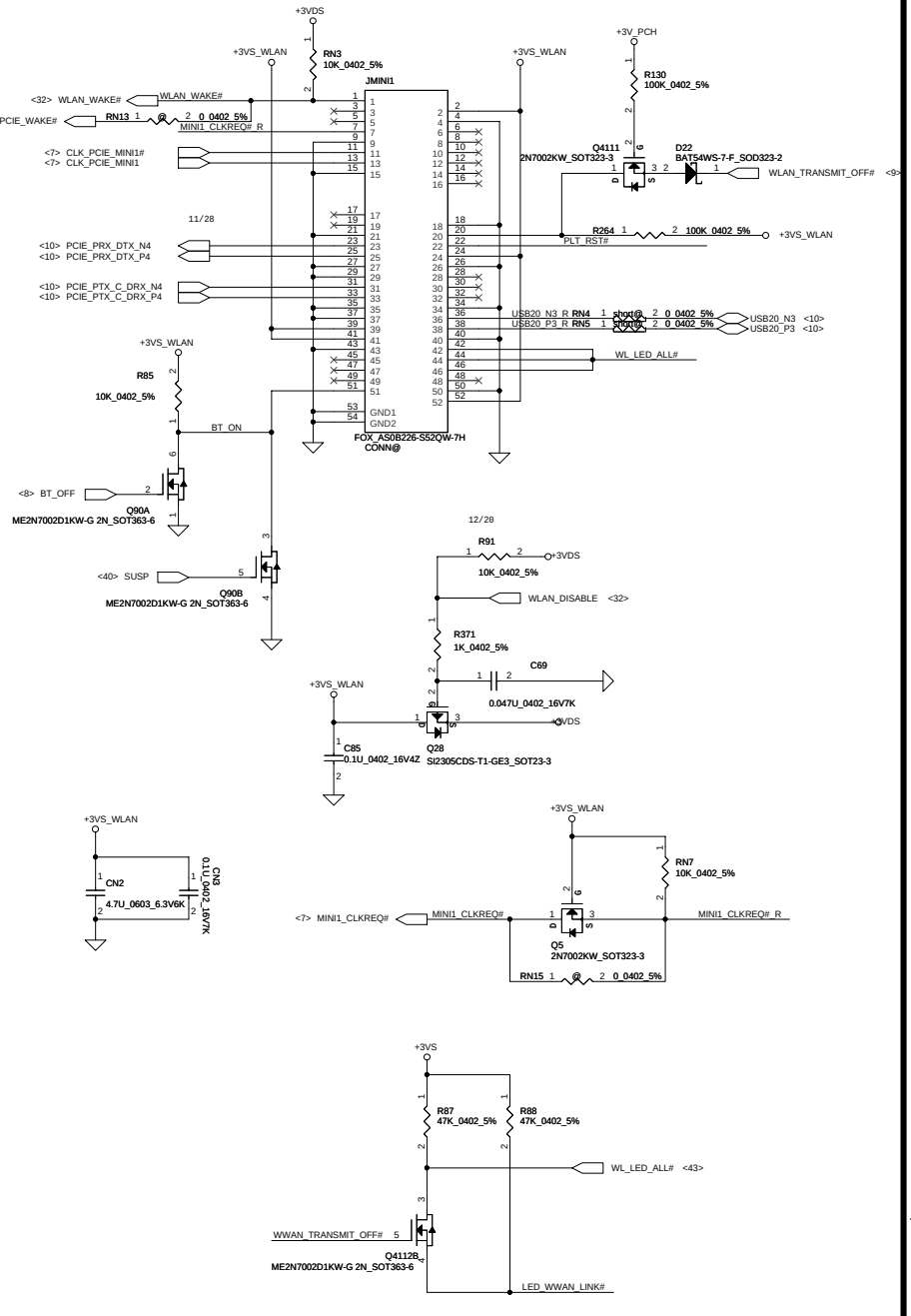
WLAN



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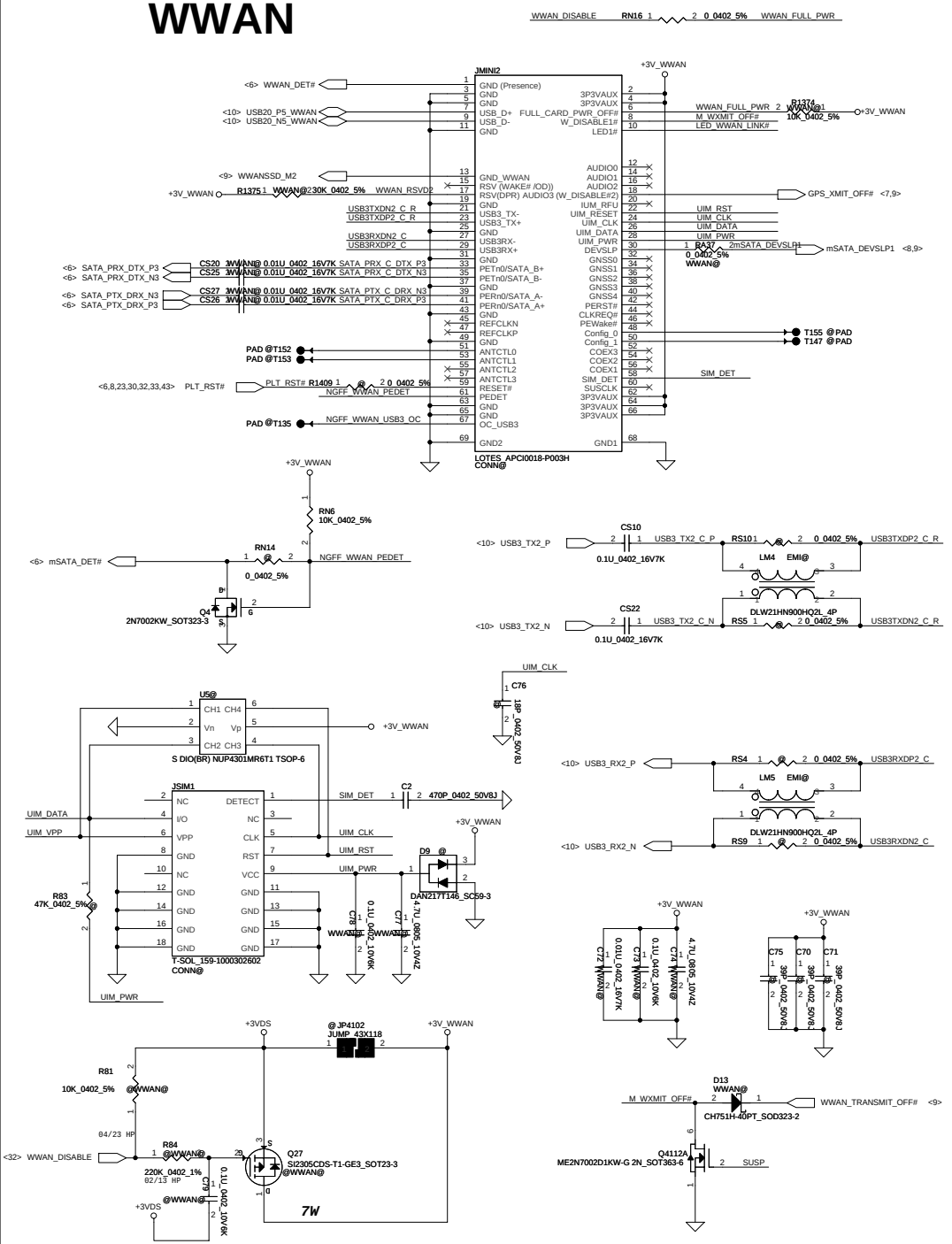

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: **WLAN**

Size	Document Number	Rev
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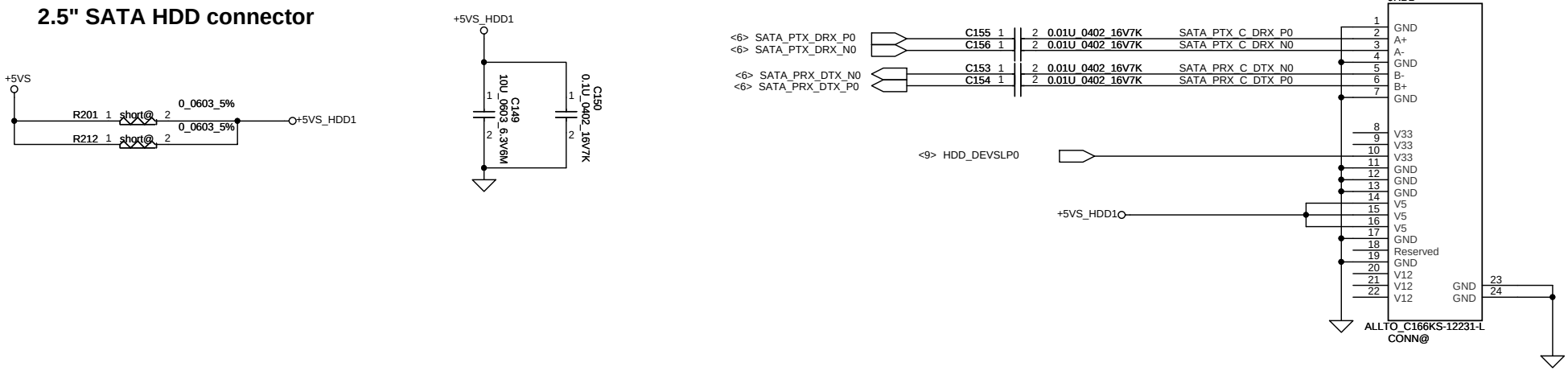
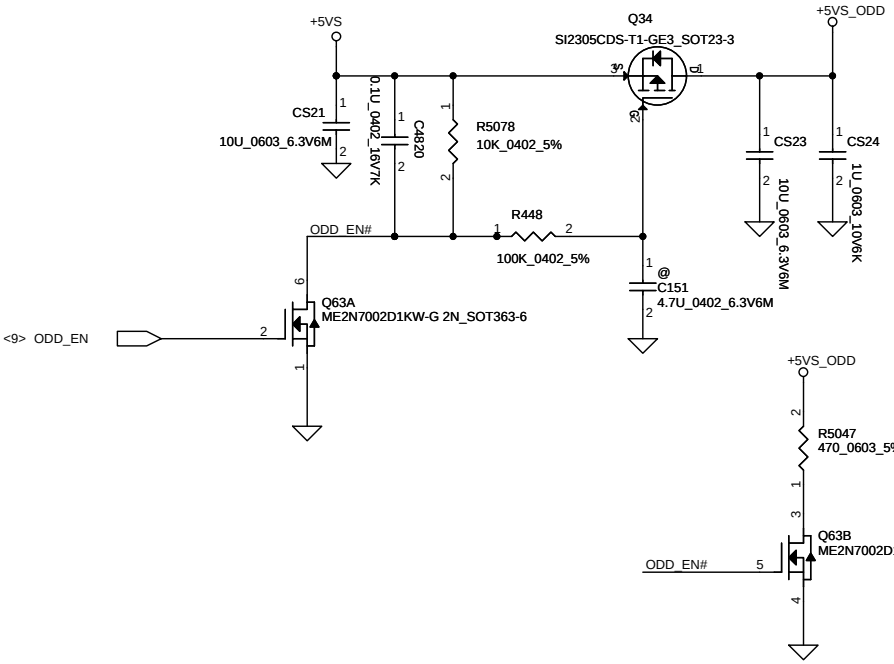
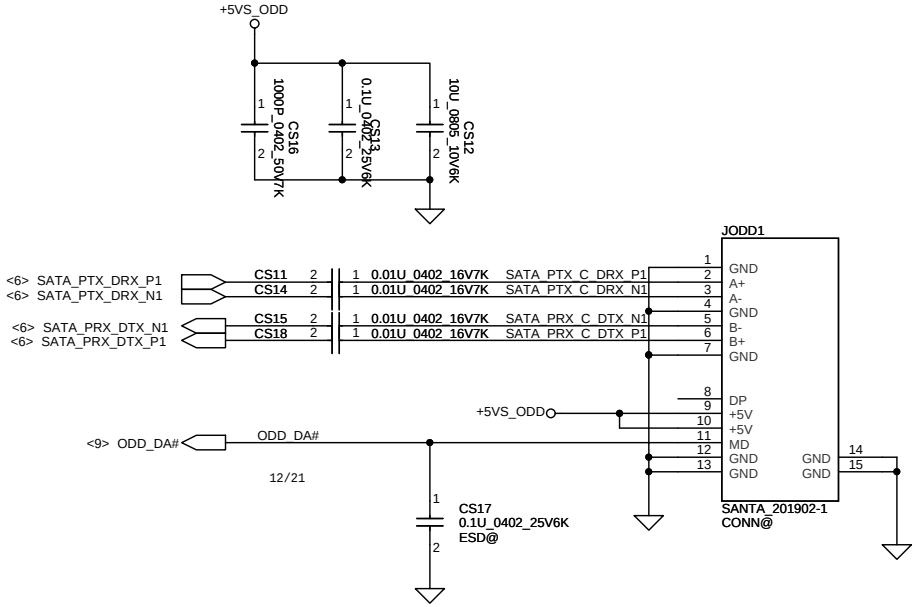
Date: Tuesday, March 25, 2014 | Sheet 21 of 62

2.5" SATA HDD connector





Please near ODD Connector



12/20 Customer change GPIO table

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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Compal Electronics, Inc.

Title: ODD/SATA Conn

Size: B | Document Number: LA-B181P | Rev: 0.5

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+LAN_VDD_3V3 Rising time need>0.5mS and <100mS

CL8& CL9 close to UL1: Pin 23

CL22 & CL23 close to UL1: Pin 11,32

CL24 close to UL1: Pin 32

CL25 close to UL1: Pin 11

CL12 & CL13 close LL2

CL17 & CL18 close UL1 Pin22

CL19 & CL20 close UL1 Pin30

Place CL14~CL16 close UL1 Pin 3, 8 , 22

+LAN_VDD_3V3=40mil

+VDDREG=40mil

+LAN_REGOUT=60mil

SP050005L00 Footprint

RJ-45 CONN.

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2011/06/29

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Compal Electronics, Inc.

Title: **LAN RTL8161GSH**

Size: | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 23 of 62

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Title

Card Reader RTS5237

Size	Document Number	Rev
Custom	LA-B181P	0.5

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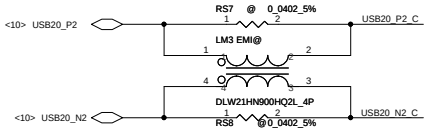
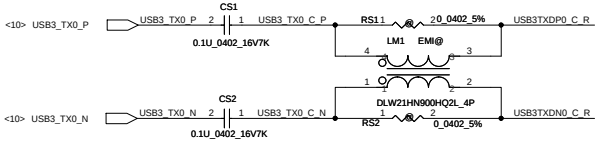
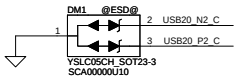
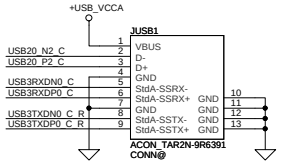
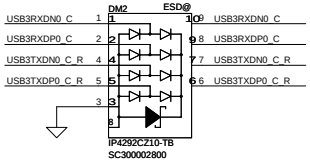
USB3.0

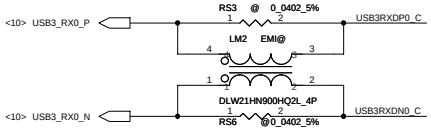




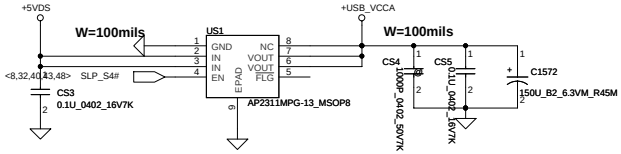


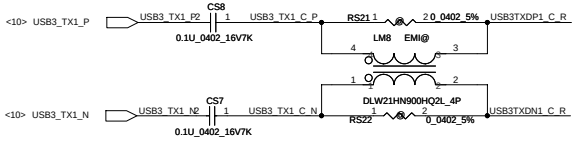


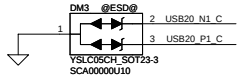


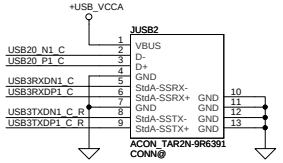


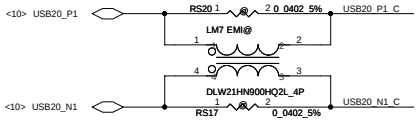
USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

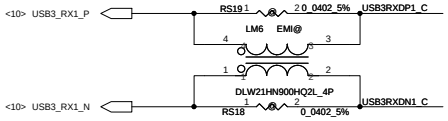


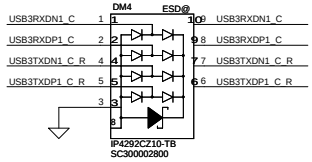




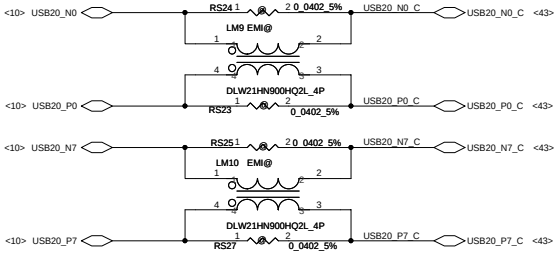








USB2.0



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Issued Date	2013/02/26	Deciphered Date	2015/07/08

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Title	USB 3.0		
Size C	Document Number LA-B181P		Rev 0.5
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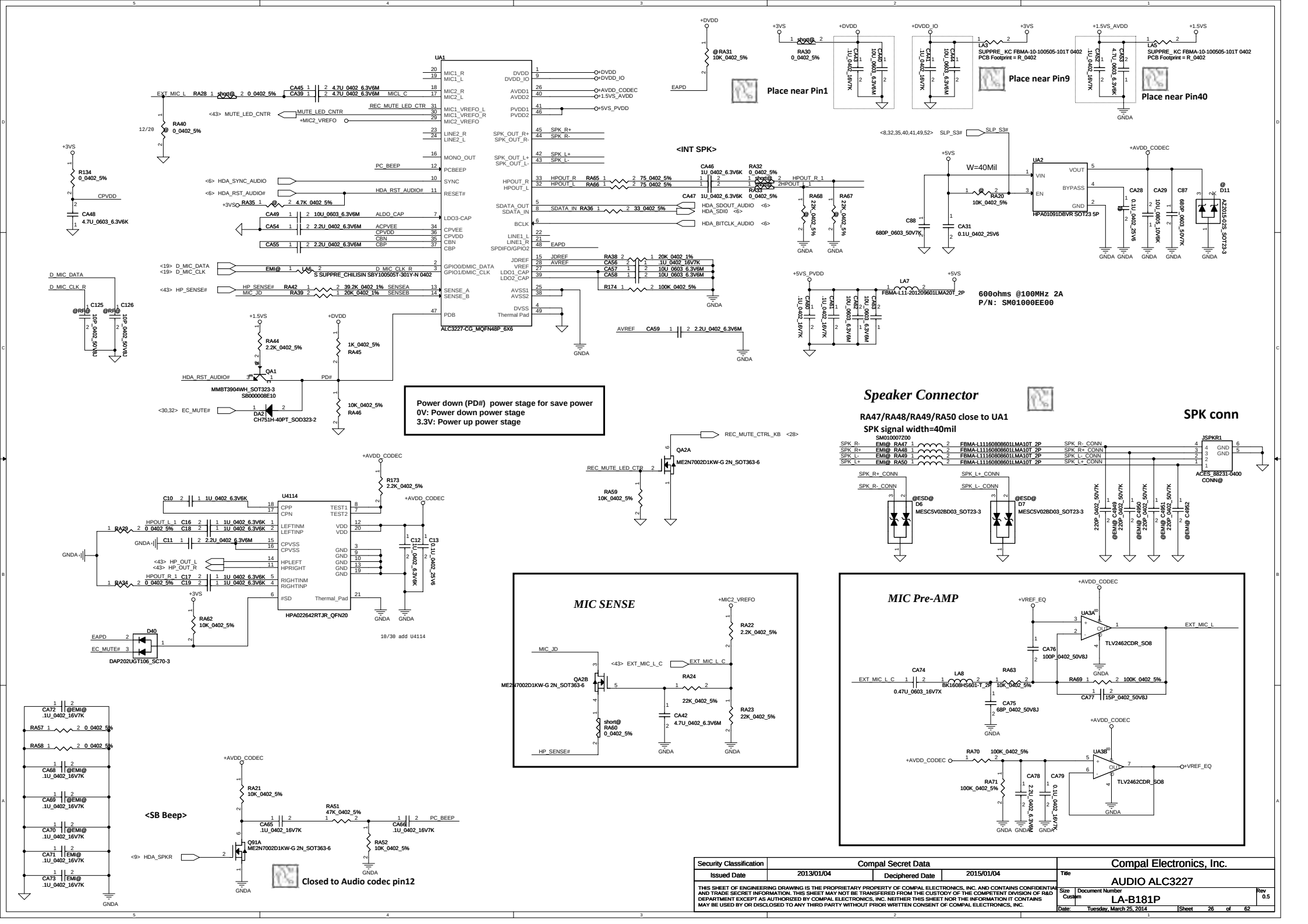

Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

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Compal Electronics, Inc.

Title: AUDIO ALC3227

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 26 of 62

Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2012/10/21

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Compal Electronics, Inc.

Title: Audio SPK Conn/Jack/MIC

Size	Document Number	Rev
C	LA-B181P	0.5

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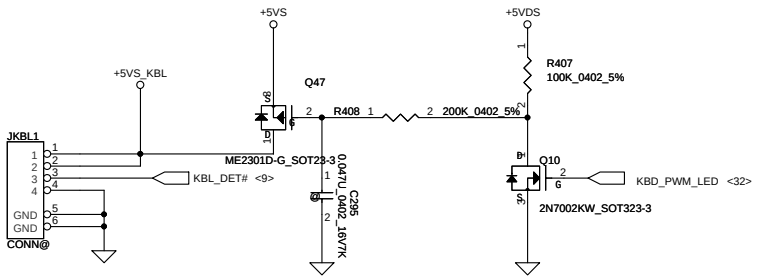
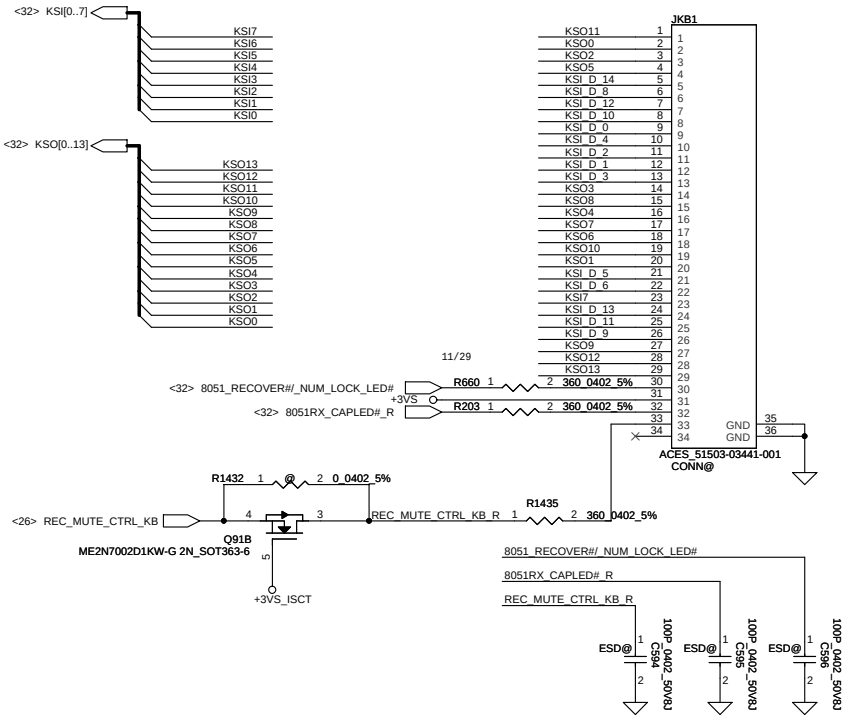
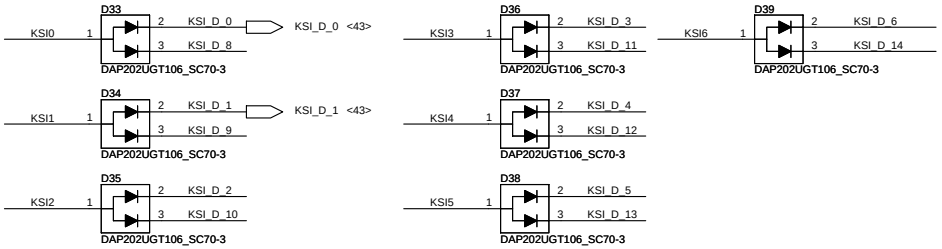
KB backlight Conn



Keyboard conn





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: KB/TP
				Size: Custom; Document Number: LA-B181P; Rev: 0.5
				Date: Tuesday, March 25, 2014; Sheet 28 of 62

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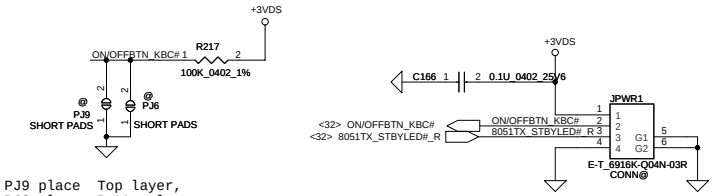
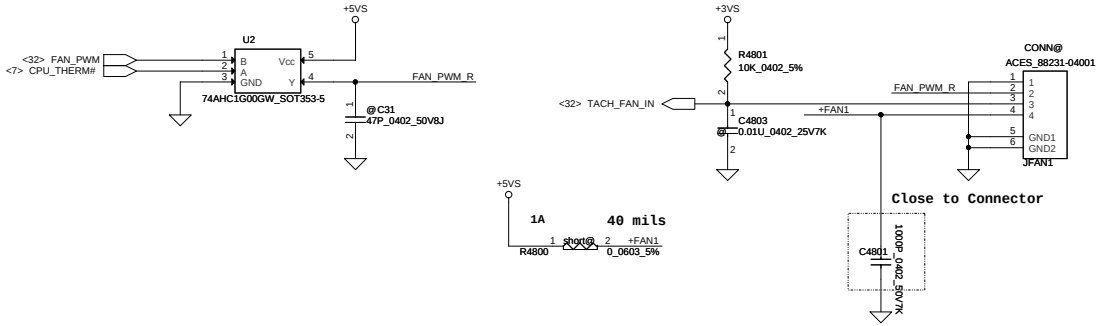
Power Button Connector



PJ9 place Top layer,
PJ6 place Bottom layer

Fan Control Circuit



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08
			Title: PWRBTN/FAN
			Size: Custom; Document Number: LA-B181P; Rev: 0.5
			Date: Tuesday, March 25, 2014; Sheet 29 of 62

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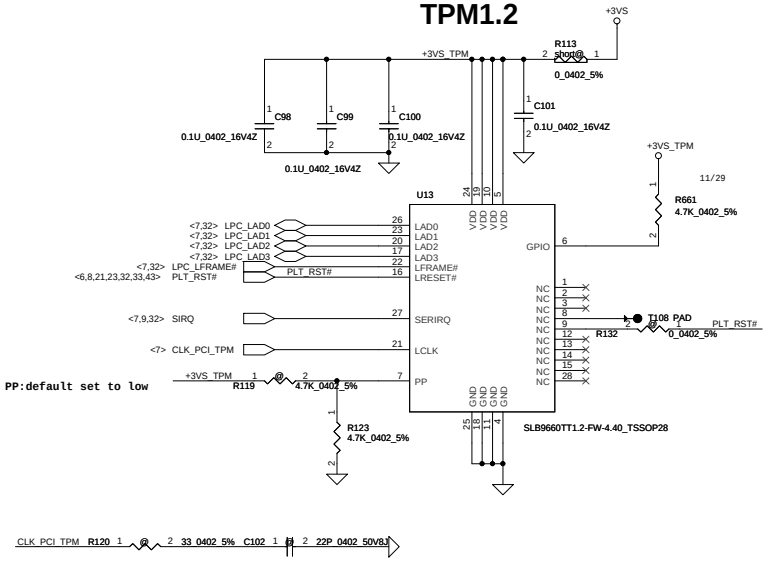
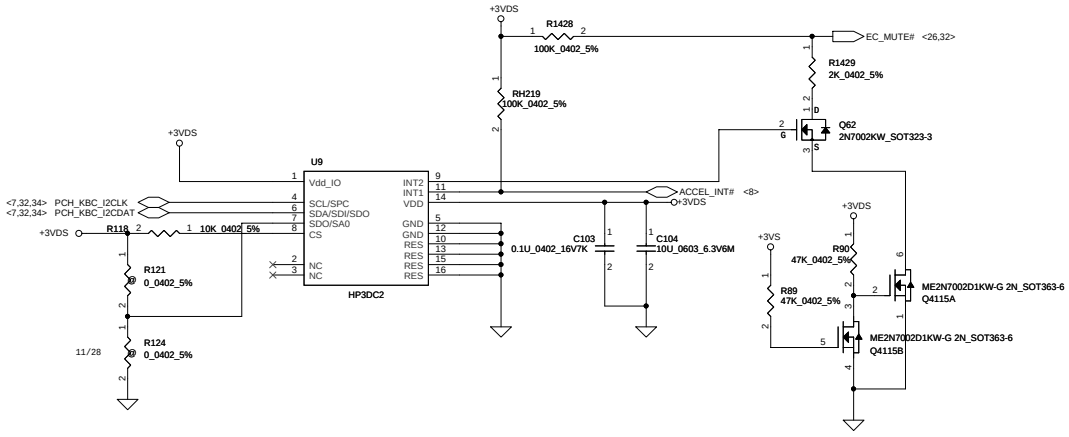
TPM1.2

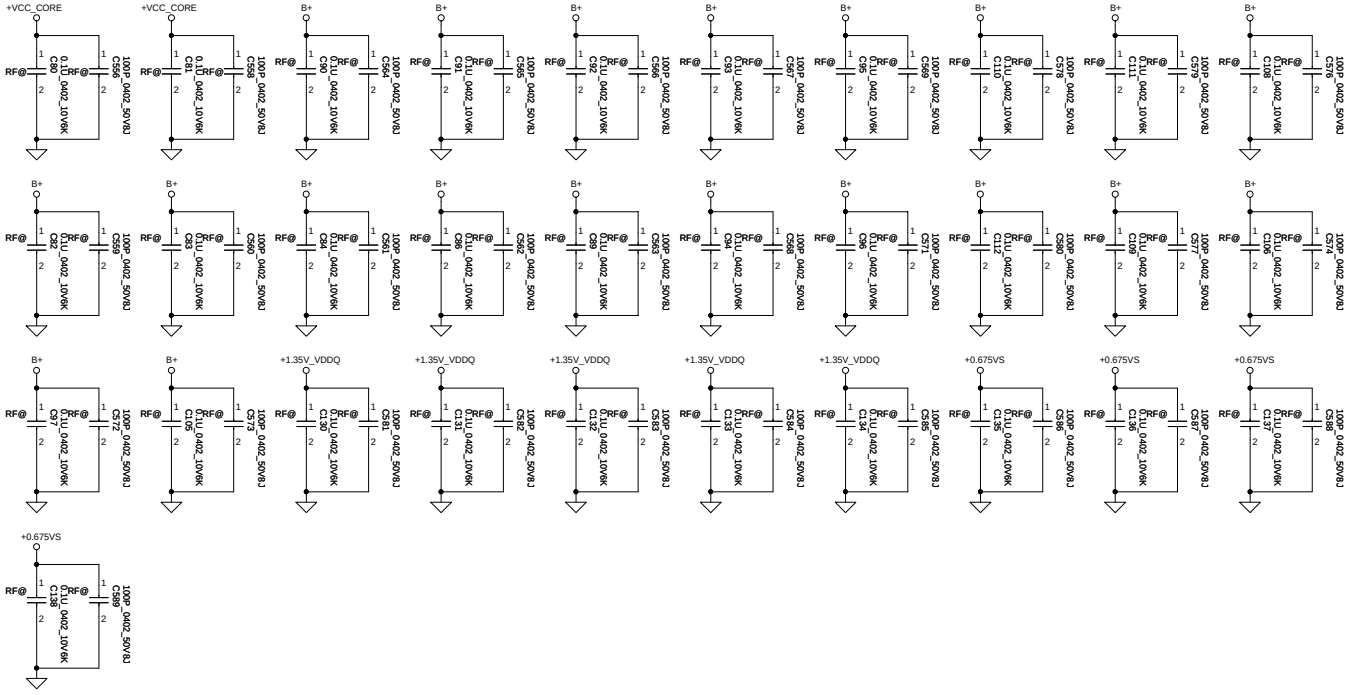


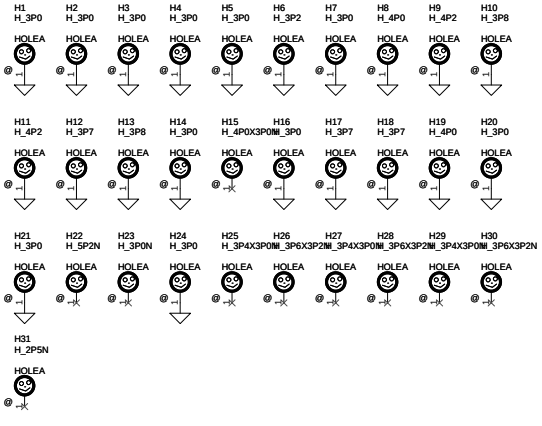
CLK_PCI_TPM R120 @ 33_0402_5% C102 @ 22P_0402_50V8J

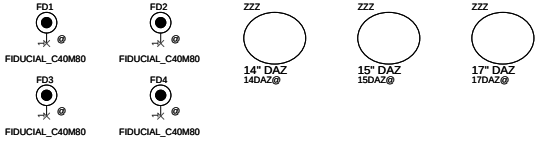
ACCELEROMETER



RF CAP







Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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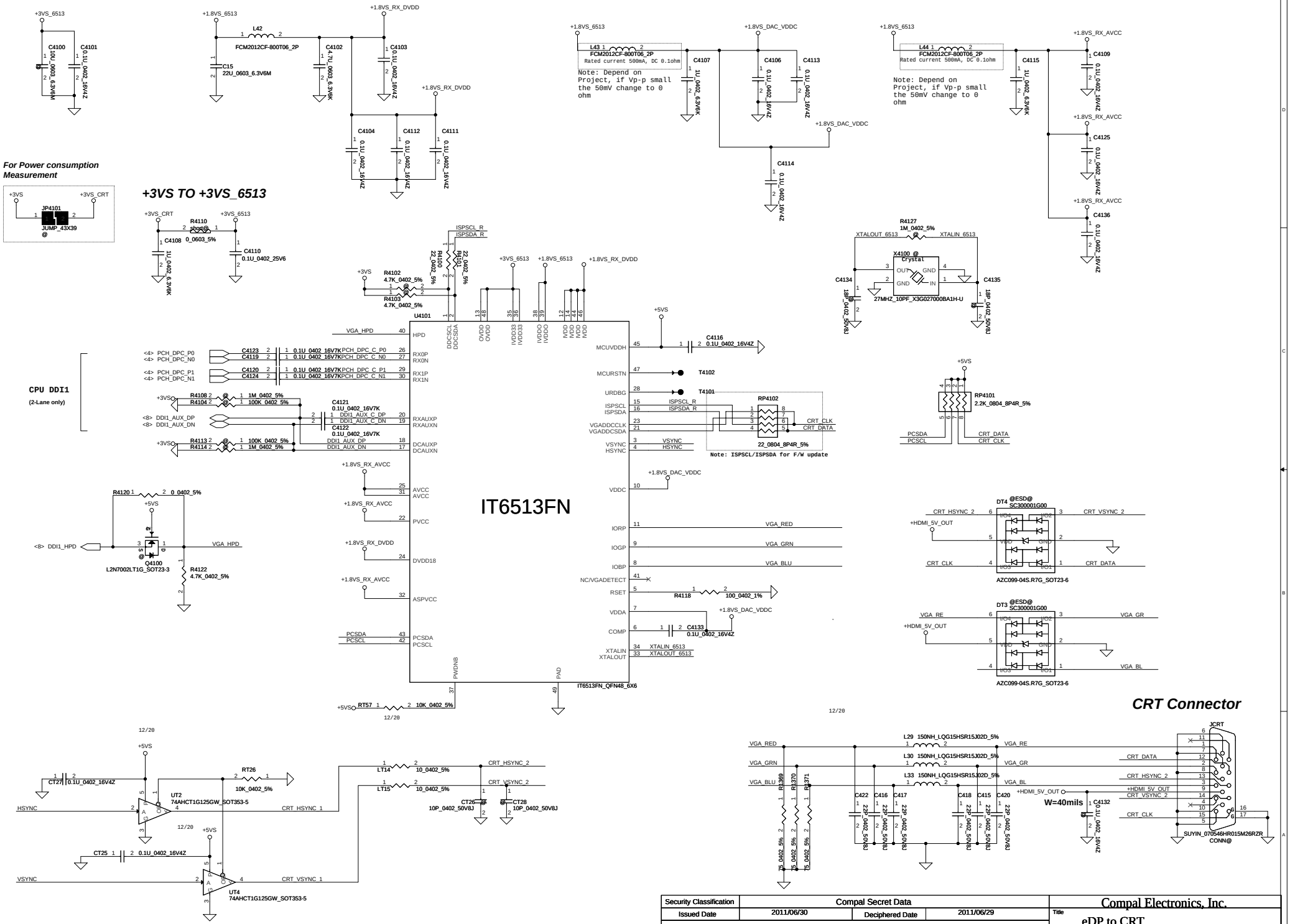
Compal Electronics, Inc.			
Title	LED/Screw hole		
Size	Document Number		Rev
	LA-B181P		0.5
Date:	Tuesday, March 25, 2014	Sheet	30 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2011/06/29

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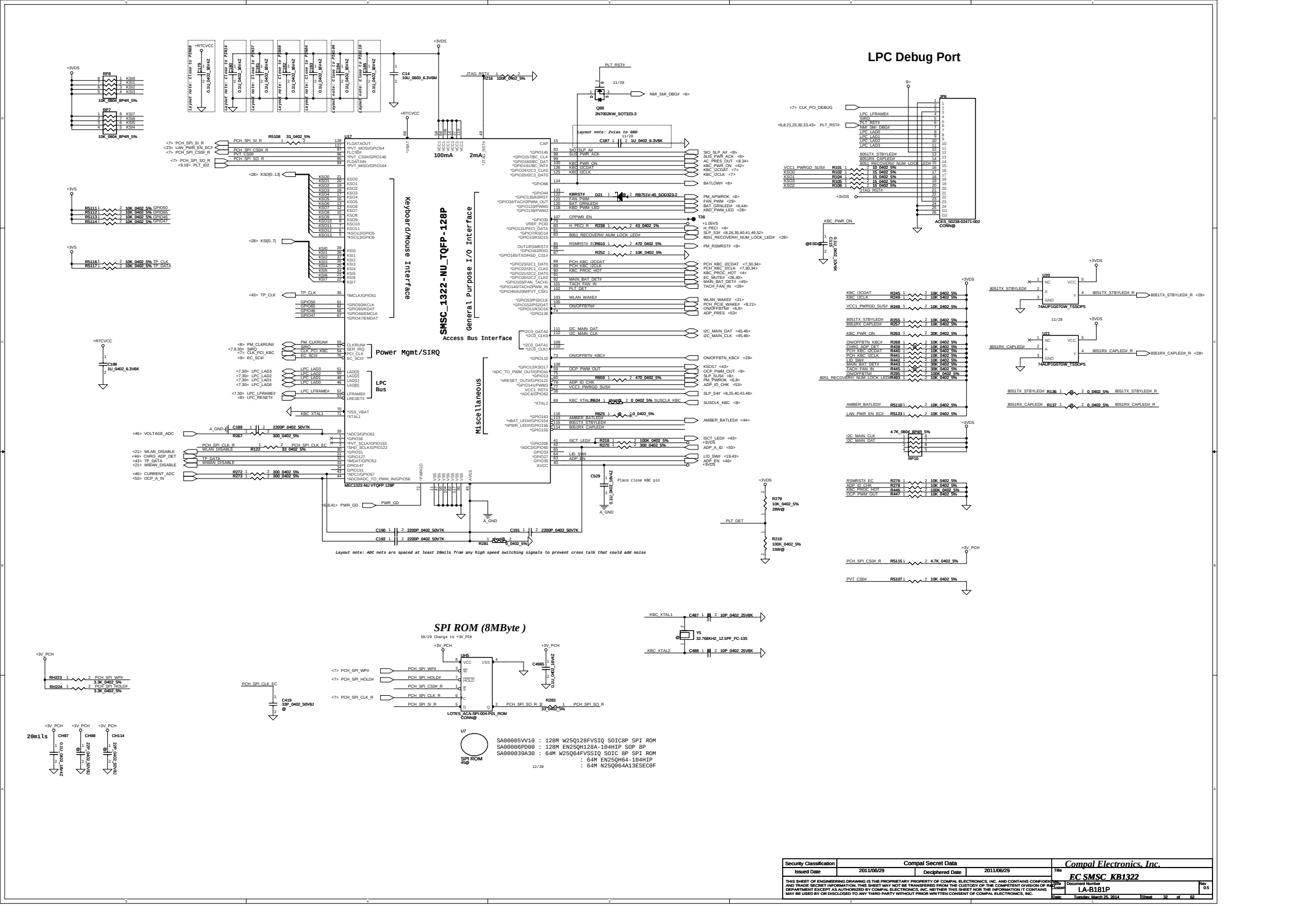
Compal Electronics, Inc.

Title: eDP to CRT

Size	Document Number	Rev
C	LA-B181P	0.5

Date: Tuesday, March 25, 2014 | Sheet 31 of 62


LPC Debug Port
SMSC_1322-NU_TQFP-128P
Keyboard/Mouse Interface
General Purpose I/O Interface
Access Bus Interface
Power Mgmt/SIRQ
LPC Bus
Miscellaneous
MEC1322-NU VTQFP 128P
SPI ROM (8MByte)
10/29 Change to +3V_PCH
LOTES_ACA-SPI-004-F01_ROM
SA00005VV10 : 128M W25Q128FVSIQ SOIC8P SPI ROM
SA00006PD00 : 128M EN25QH128A-104HIP SOP 8P
SA00039A30 : 64M W25Q64FVSSIQ SOIC 8P SPI ROM
: 64M EN25QH64-104HIP
: 64M N25Q064A13ESEC0F
Layout note: ADC nets are spaced at least 20mils from any high speed switching signals to prevent cross talk that could add noise
Layout note: 2vias to GND
Place close KBC pin
Security Classification
Compal Secret Data
Issued Date
2011/06/29
Deciphered Date
2011/06/29
Compal Electronics, Inc.
EC SMSC KB1322
Document Number
LA-B181P
Rev
0.5
Date: Tuesday, March 25, 2014
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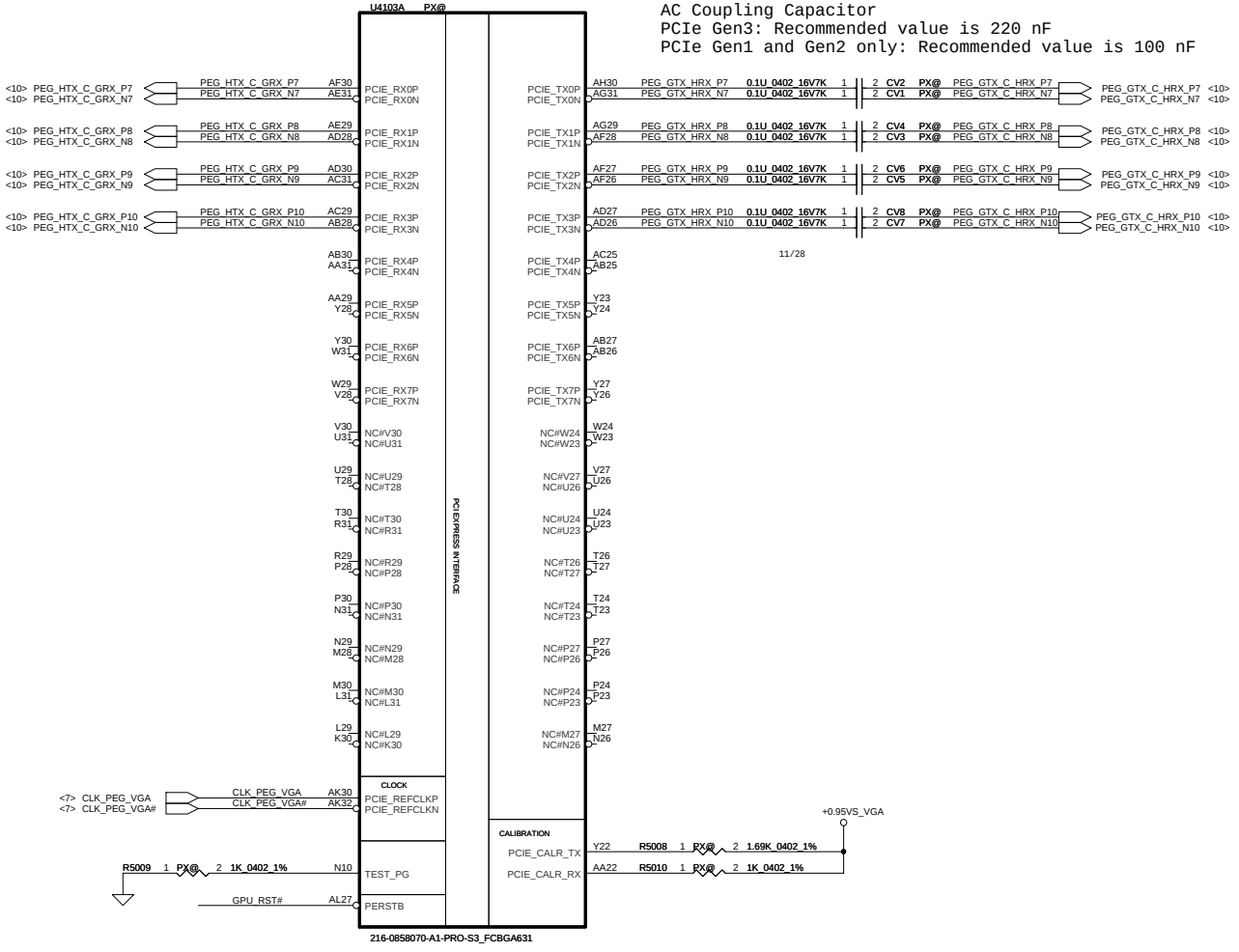
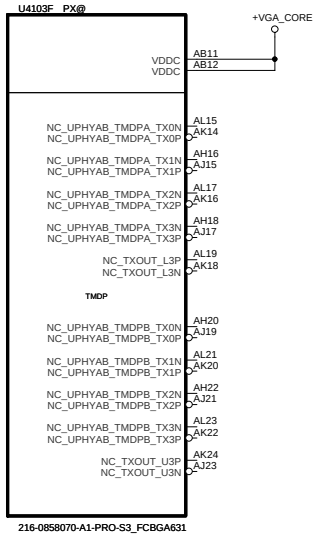
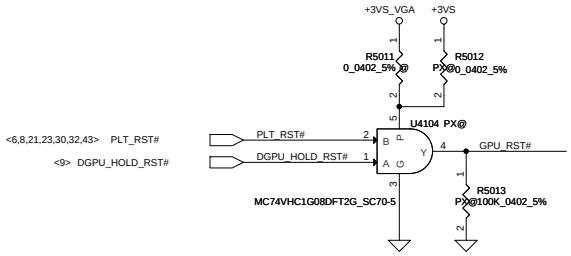
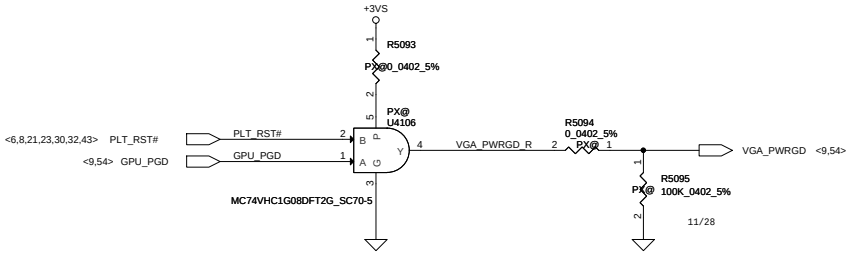
AC Coupling Capacitor
PCIe Gen3: Recommended value is 220 nF
PCIe Gen1 and Gen2 only: Recommended value is 100 nF



No Use GPU Display Port outpud







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Issued Date	2013/01/11	Deciphered Date	2013/12/31

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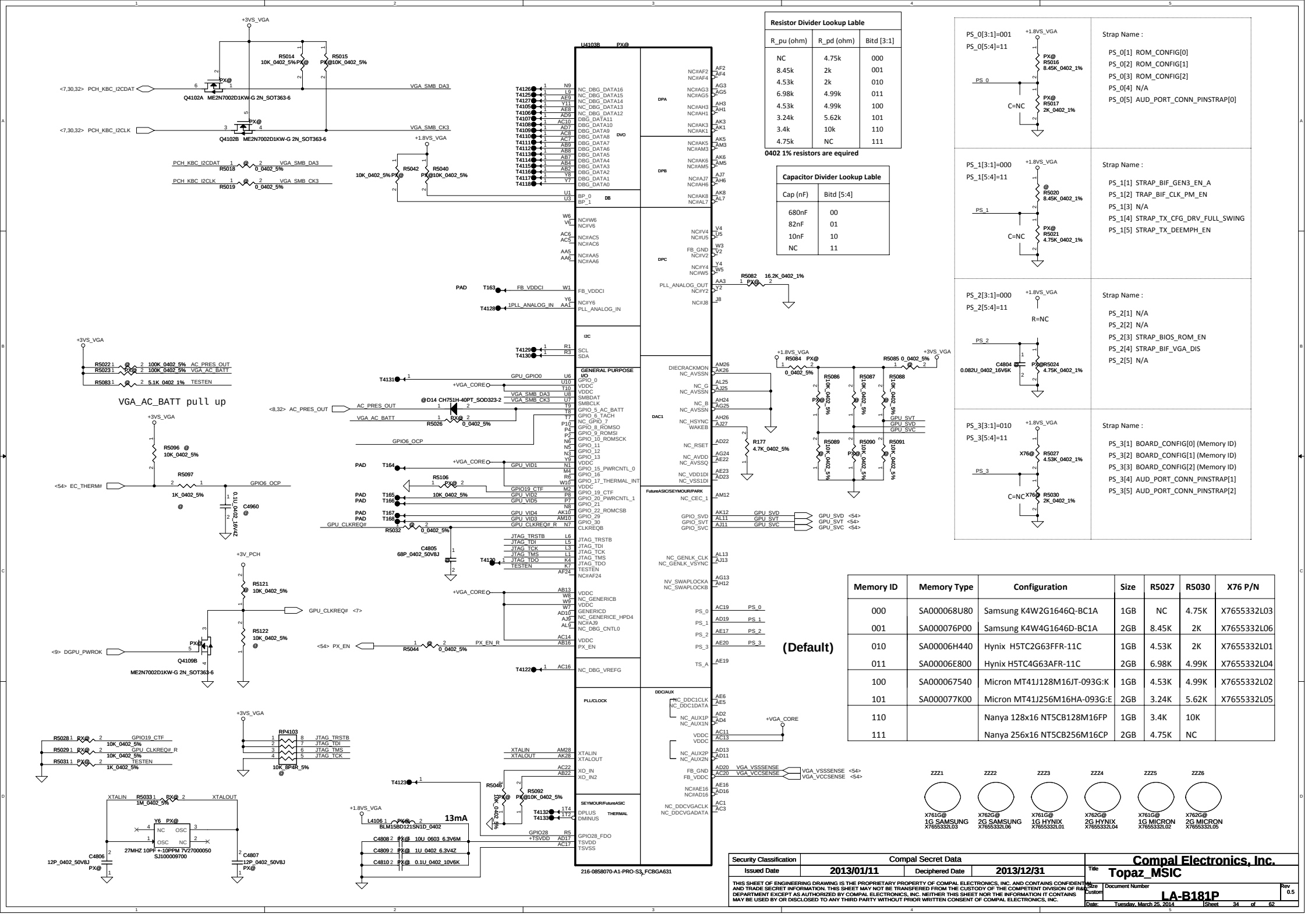
Compal Electronics, Inc.

Title	Topaz_PCIE/DP	
Size: Custom	Document Number: LA-B181P	Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 33 of 62	



Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Memory ID	Memory Type	Configuration	Size	R5027	R5030	X76 P/N
000	SA000068U80	Samsung K4W2G1646Q-BC1A	1GB	NC	4.75K	X7655332L03
001	SA000076P00	Samsung K4W4G1646D-BC1A	2GB	8.45K	2K	X7655332L06
010	SA00006H440	Hynix H5TC2G63FFR-11C	1GB	4.53K	2K	X7655332L01
011	SA00006E800	Hynix H5TC4G63AFR-11C	2GB	6.98K	4.99K	X7655332L04
100	SA000067540	Micron MT41J128M16JT-093G:K	1GB	4.53K	4.99K	X7655332L02
101	SA000077K00	Micron MT41J256M16HA-093G:E	2GB	3.24K	5.62K	X7655332L05
110		Nanya 128x16 NT5CB128M16FP	1GB	3.4K	10K	
111		Nanya 256x16 NT5CB256M16CP	2GB	4.75K	NC	

(Default)

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Compal Electronics, Inc.

Title: **Topaz_MSIC**

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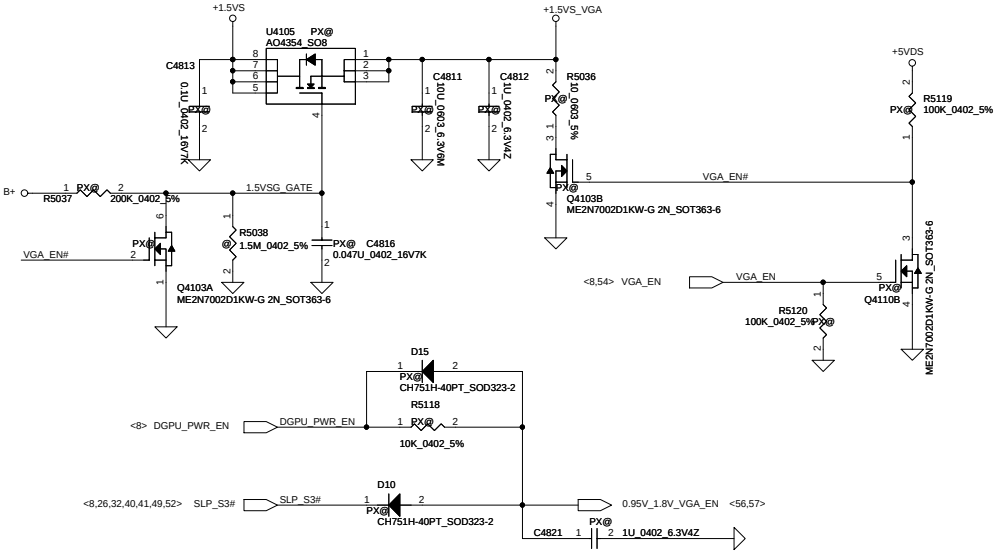
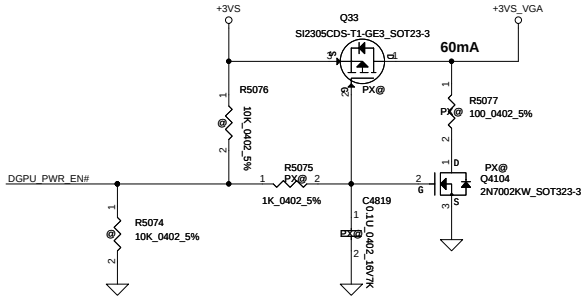
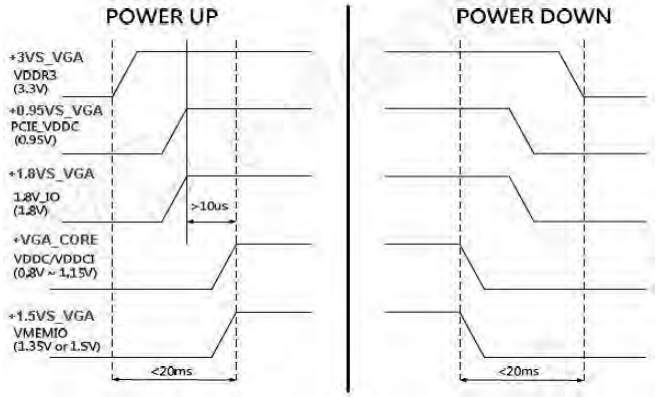
Date: Tuesday, March 25, 2014 | Sheet 34 of 62

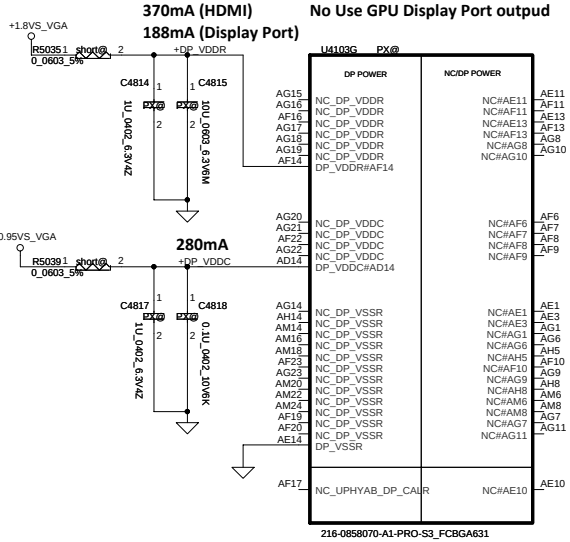
+1.5VS to +1.5VS_VGA (2.096A)

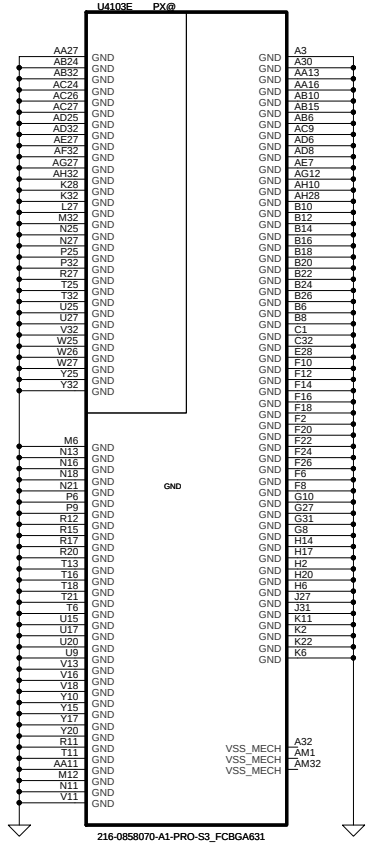


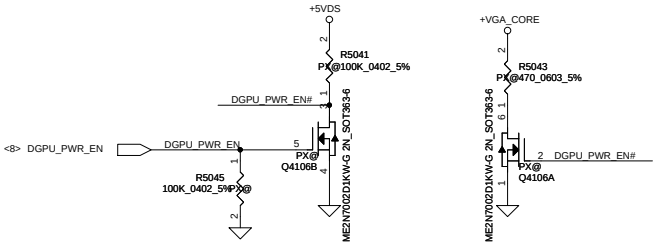
+3VS to +3VS_VGA (25mA)











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Compal Electronics, Inc.

Title: **Topaz_Power/GND**

Size: Custom | Document Number: **LA-B181P** | Rev: 0.5

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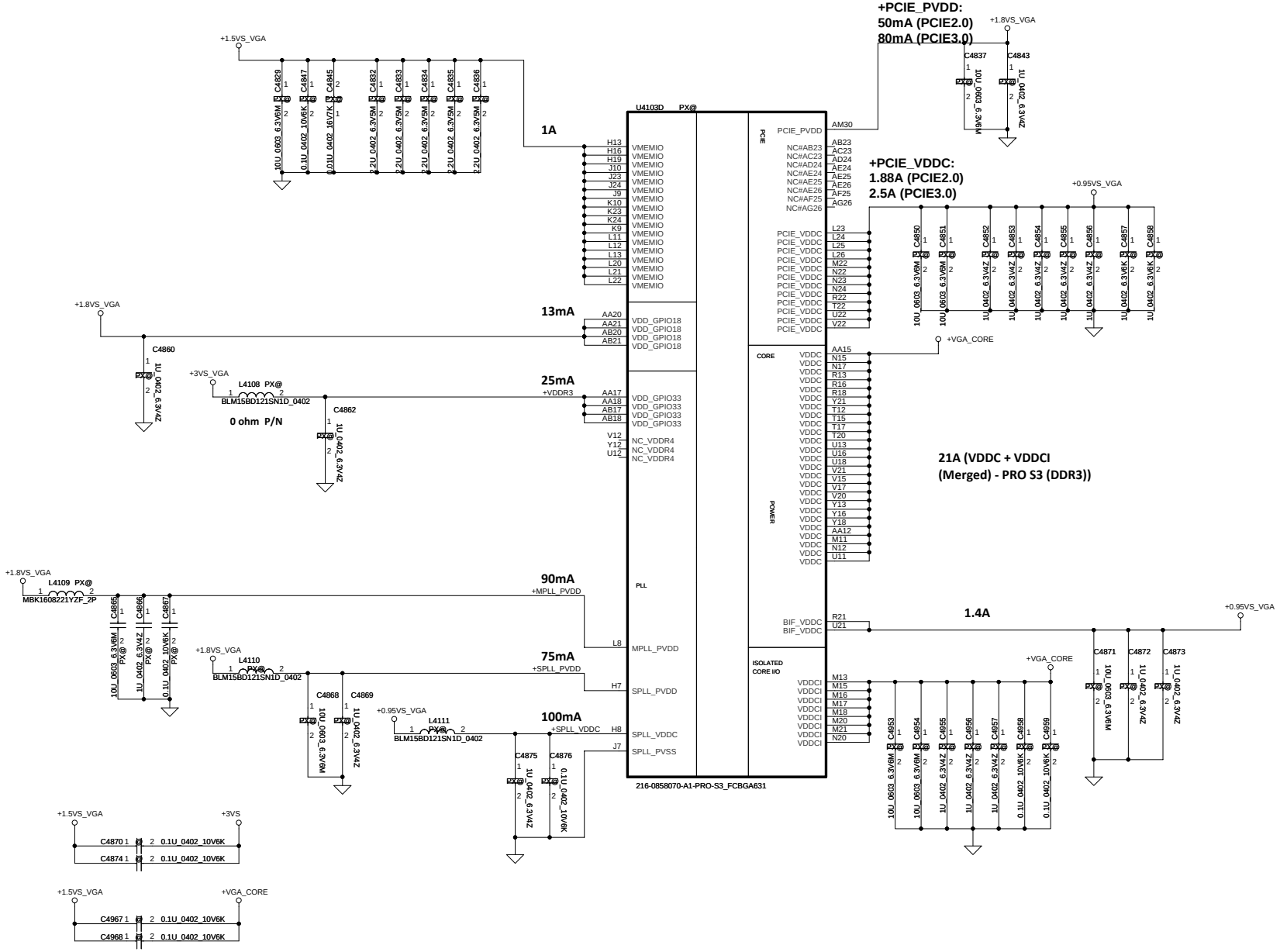
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



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Title: Topaz_Power

Size: Custom | Document Number: LA-B181P | Rev: 0.5

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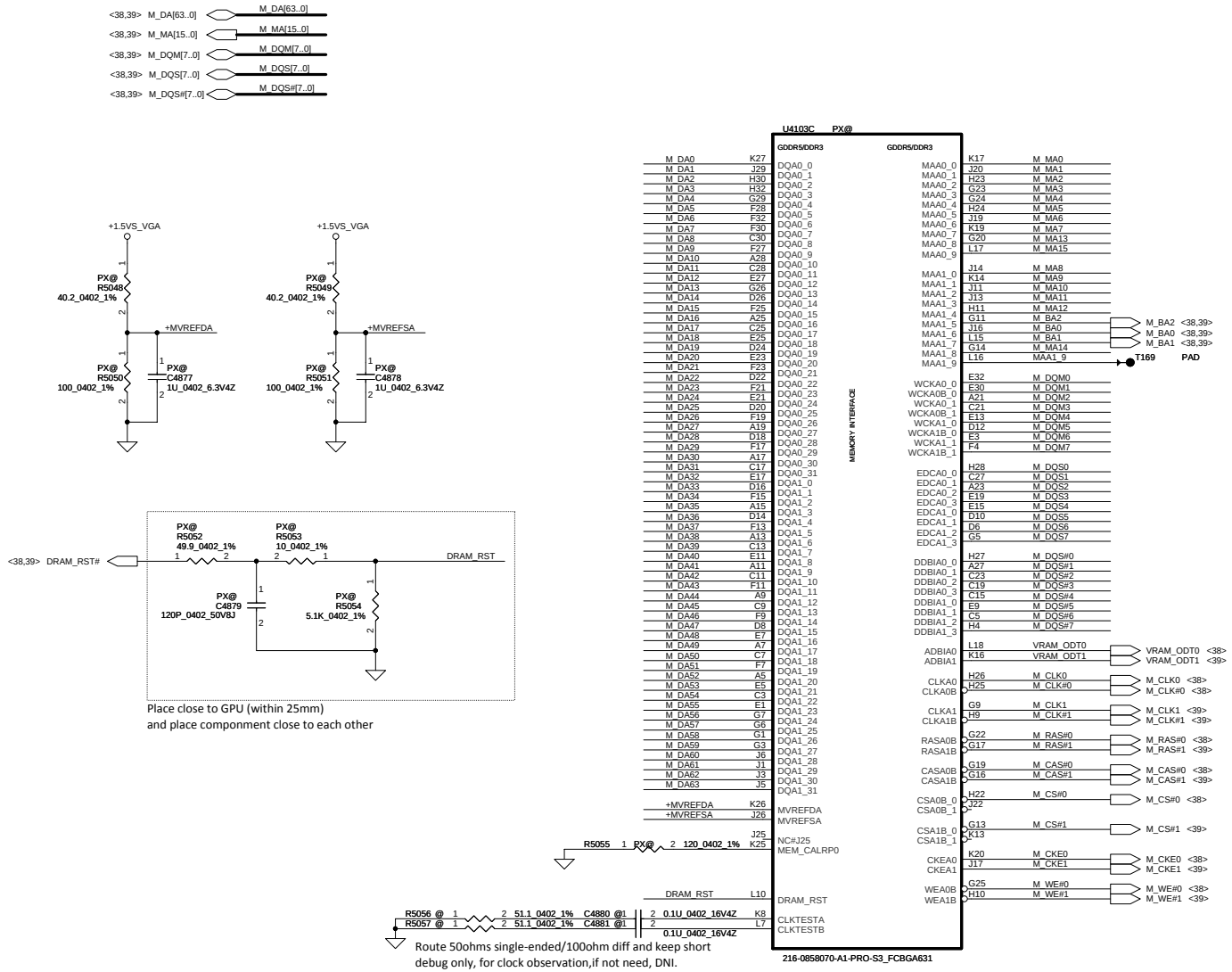

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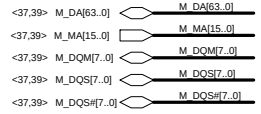
Title: Topaz_MEM

Size: Custom | Document Number: LA-B181P | Rev: 0.5

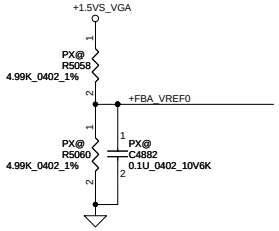
Date: Tuesday, March 25, 2014 | Sheet 37 of 62

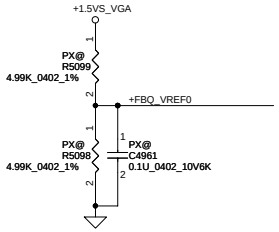
Memory Partition A - Lower 32 bits

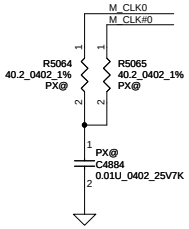


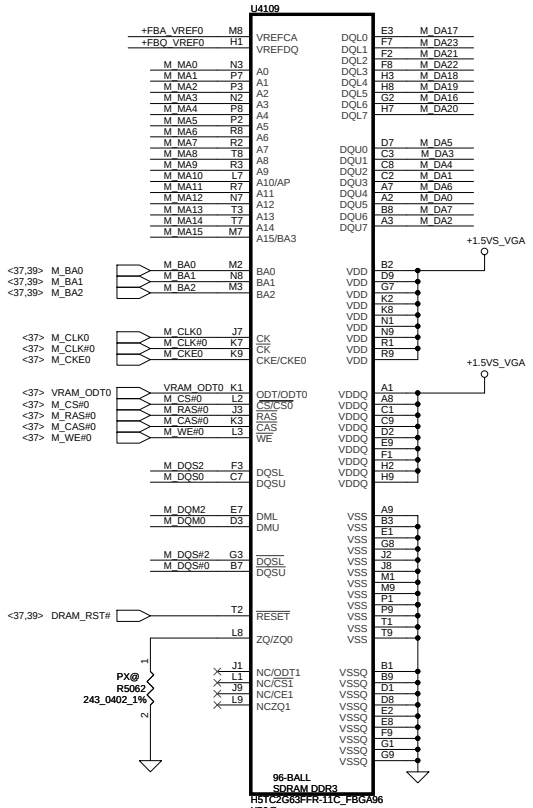
UH1 @Hynix

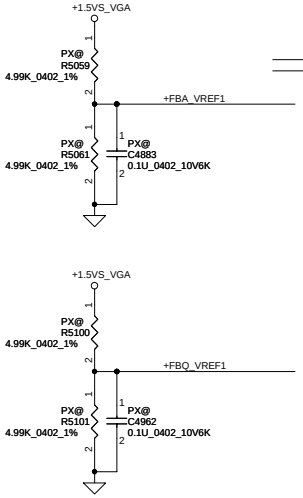
UM1 @Micron

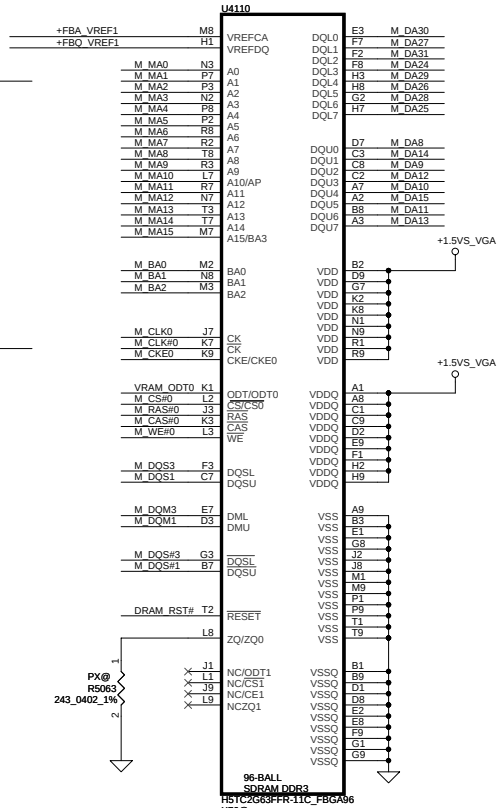


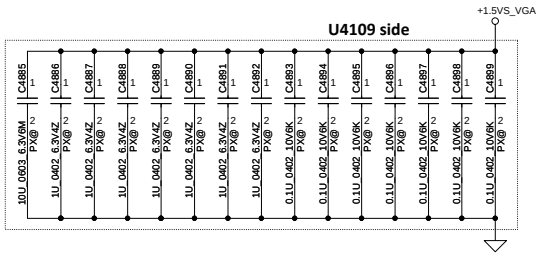


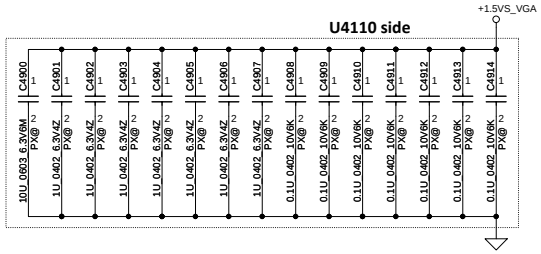












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Compal Electronics, Inc.

Title: Topaz_VRAM A Lower

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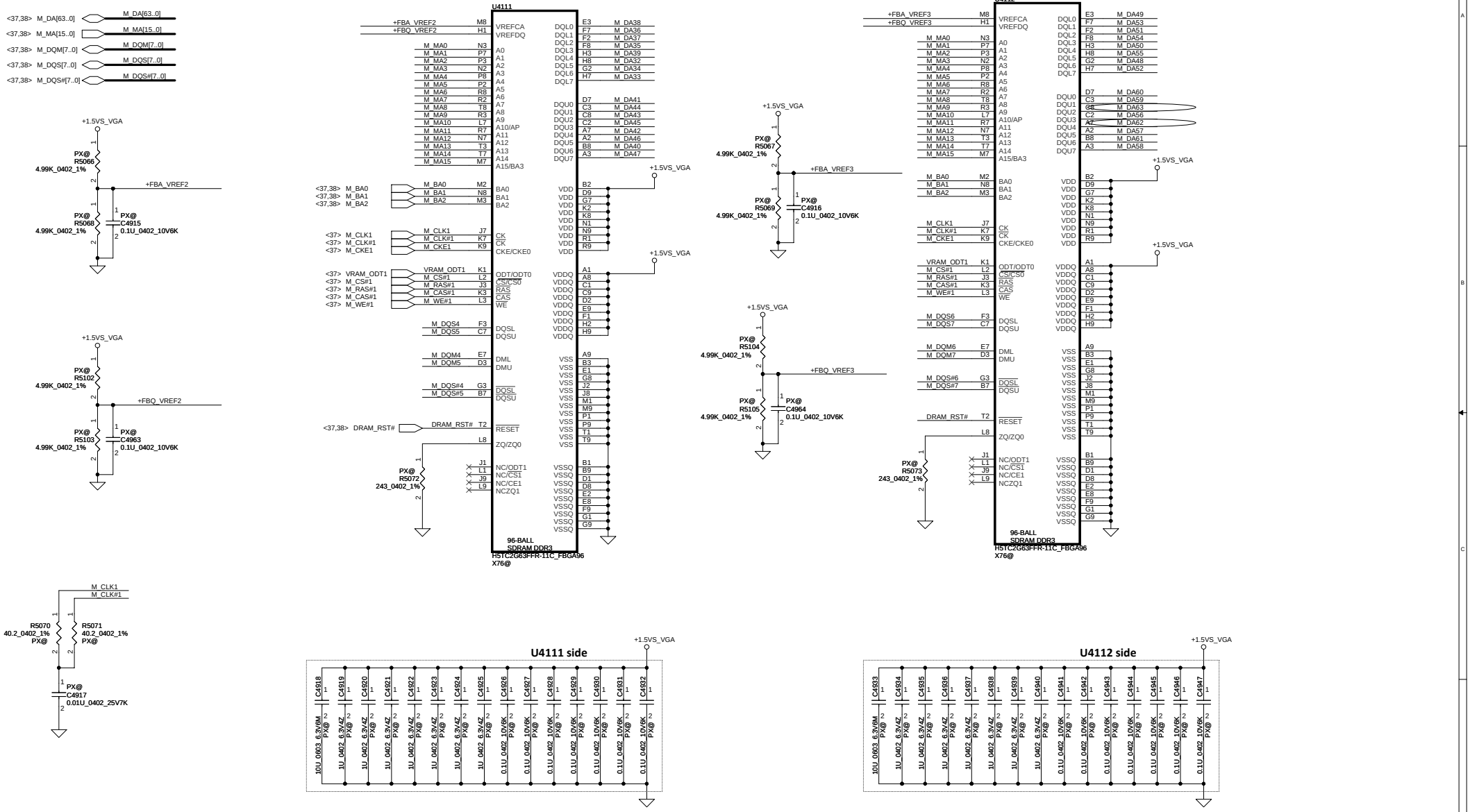
Memory Partition A - Upper 32 bits



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Title: **Topaz_VRAM A Upper**

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Custom	LA-B181P	0.5

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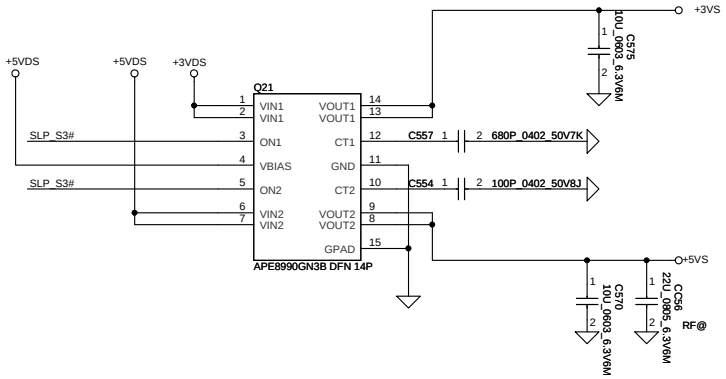
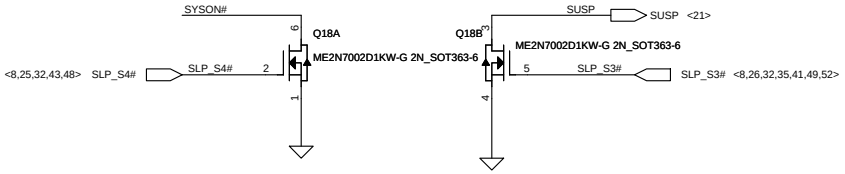
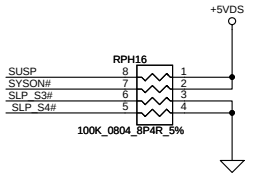
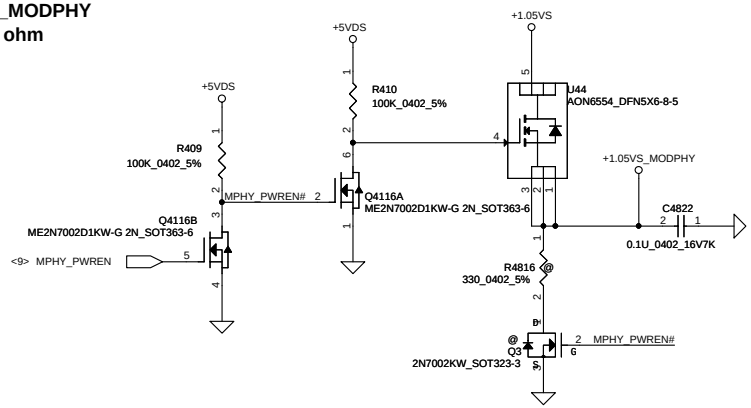






CPU +V1.05DX_MODPHY
Max Rdson <6m ohm
1840mA



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-B181P	0.5

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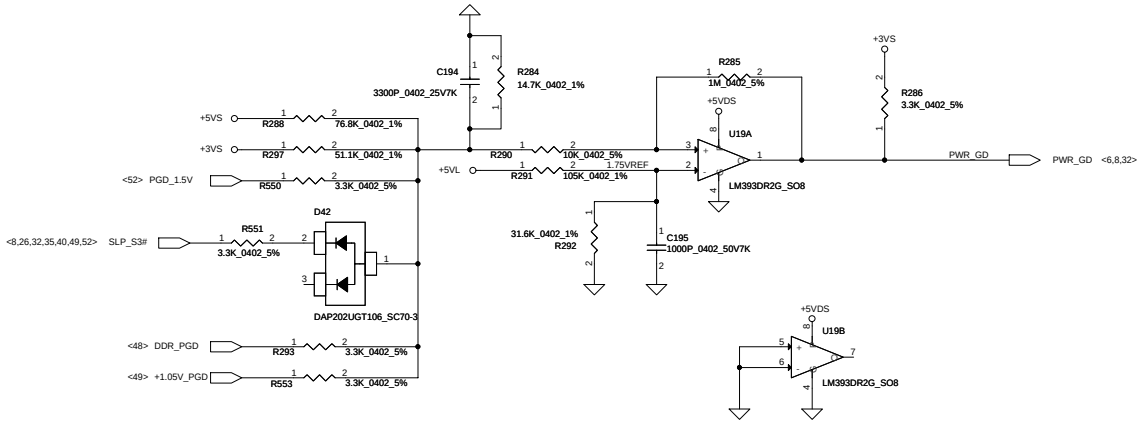

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Title	WAKE and RST-1	
Size: C	Document Number: LA-B181P	Rev: 0.5
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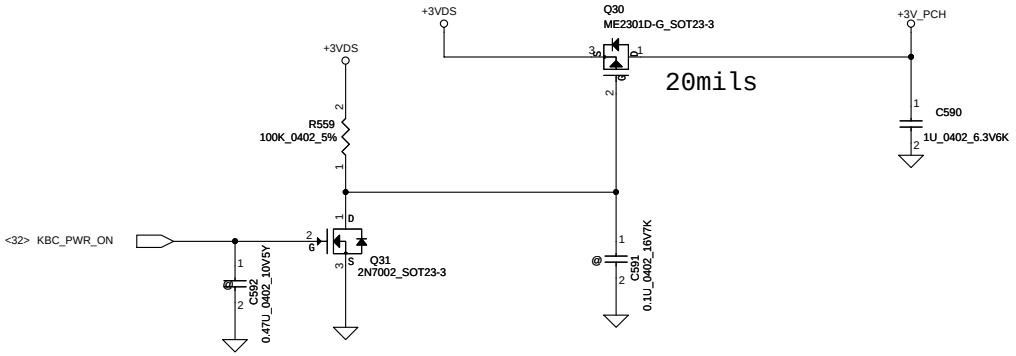

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Compal Electronics, Inc.

Title: DC DC Device-1

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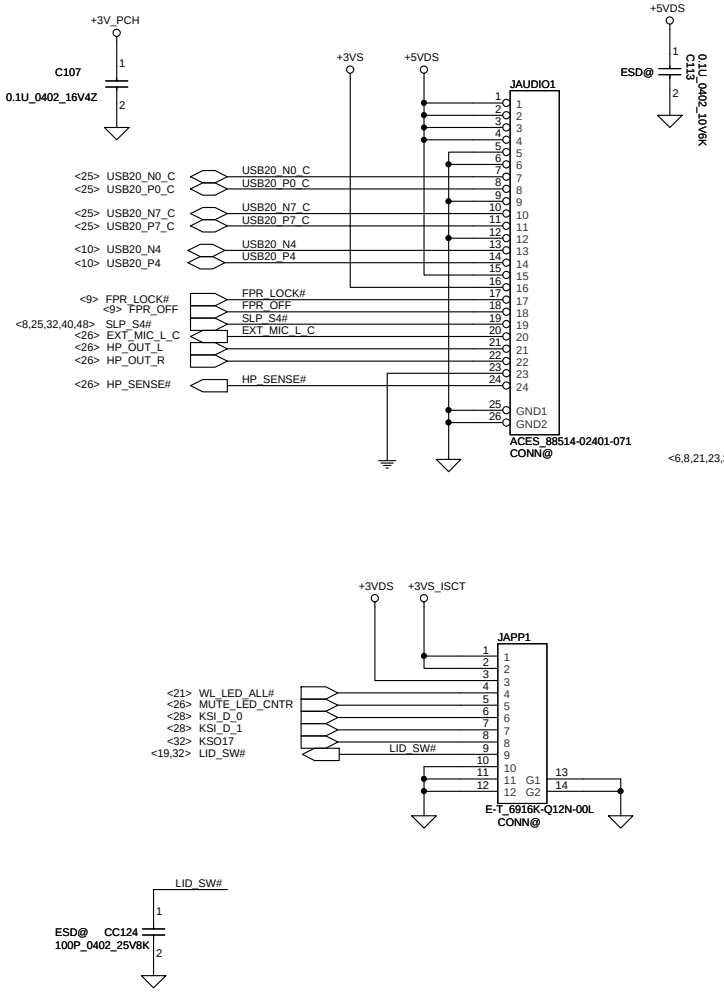
Audio Board

USB CONN

Finger printer

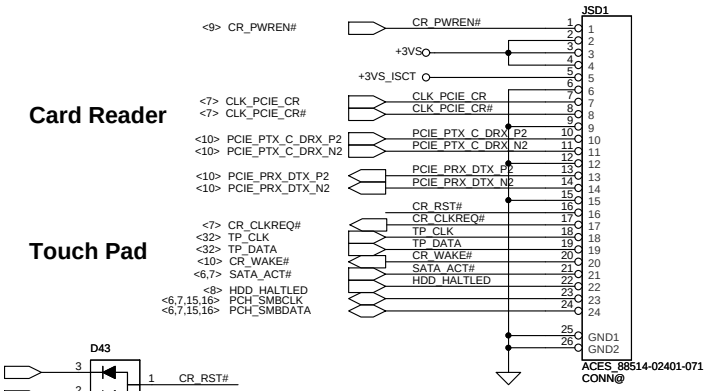
Combo Jack

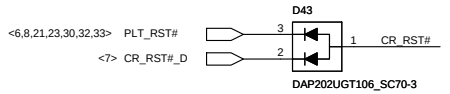


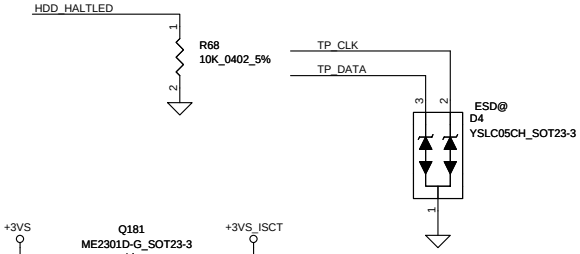
Card Reader Board

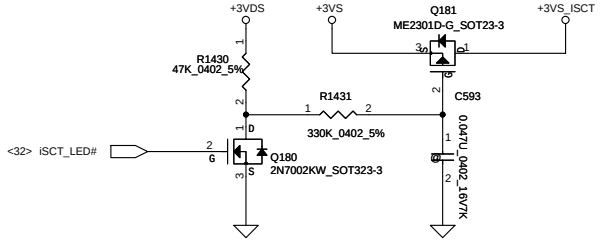
Card Reader

Touch Pad









Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DC DC Device-1

Size	Document Number	Rev
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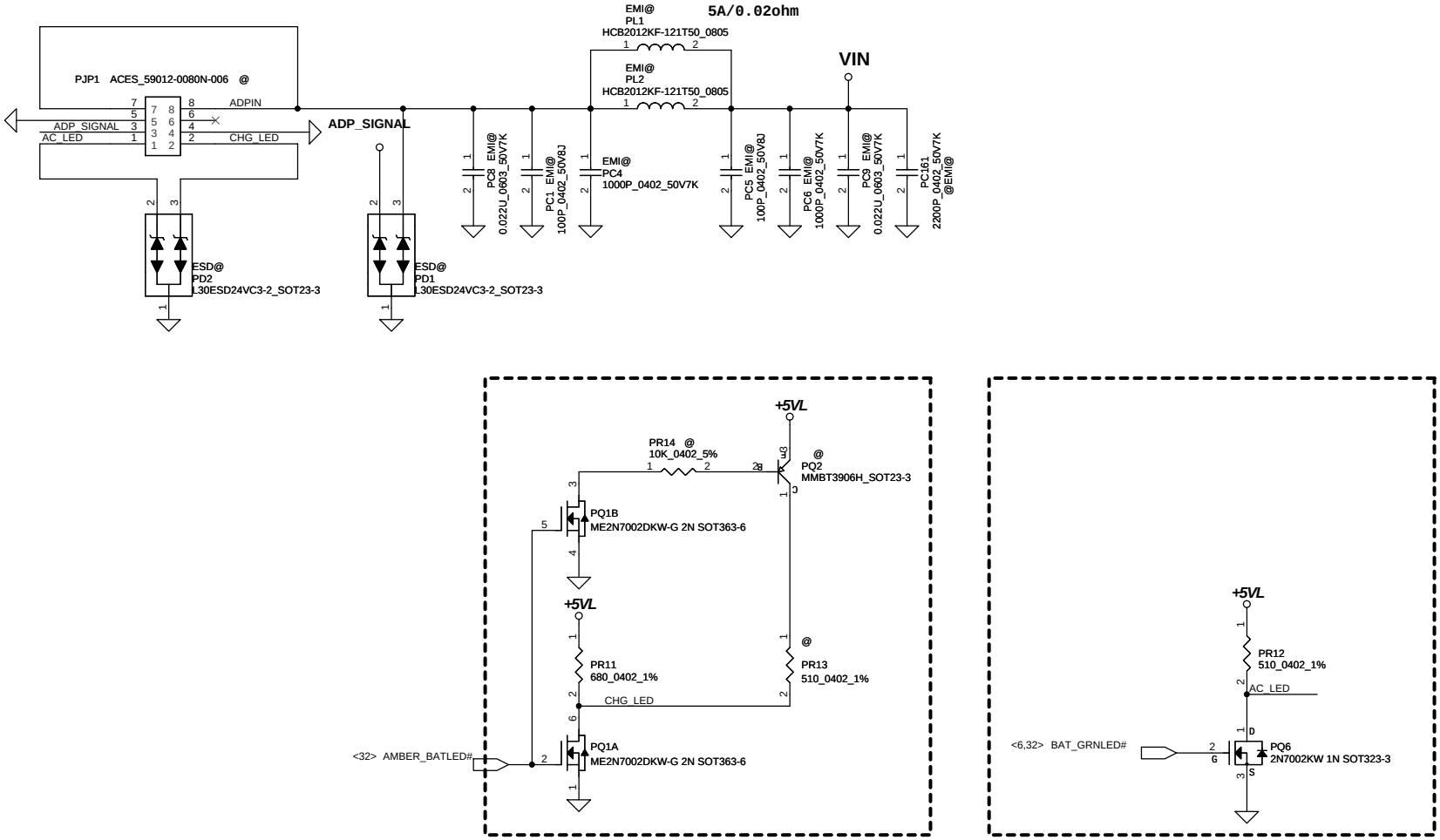

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Issued Date	2013/09/09	Deciphered Date	2016/09/30

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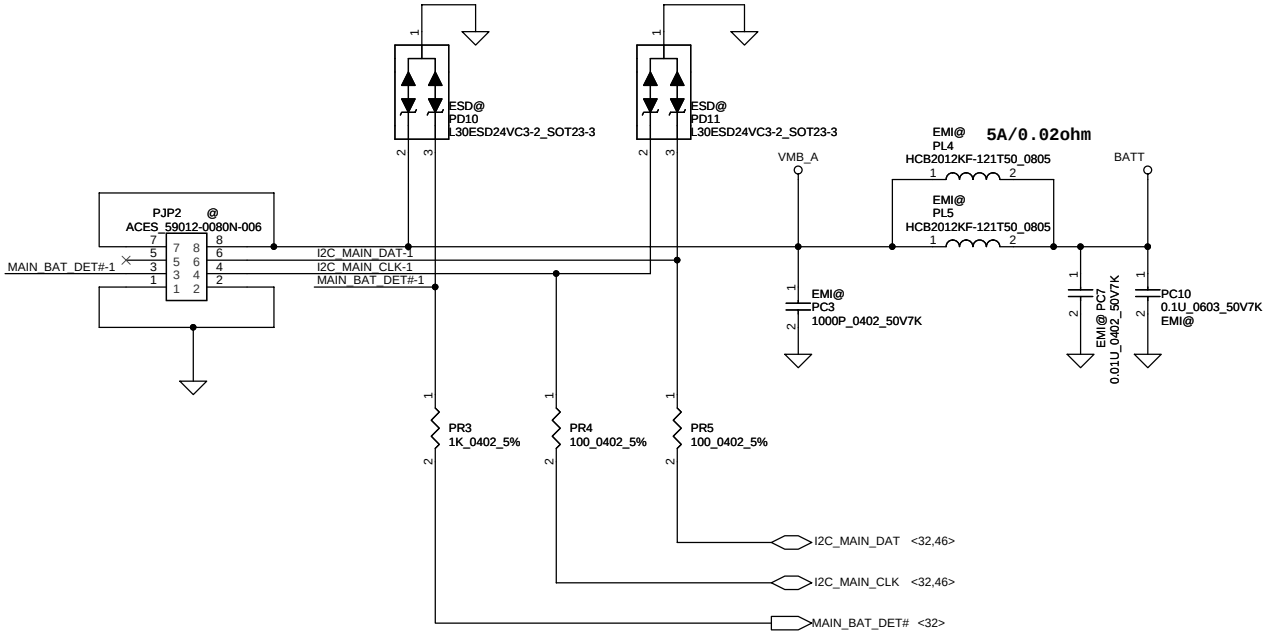
Compal Electronics, Inc.

Title: ***DC Conn***

Size | Document Number: **LA-B181P** | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 44 of 62



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

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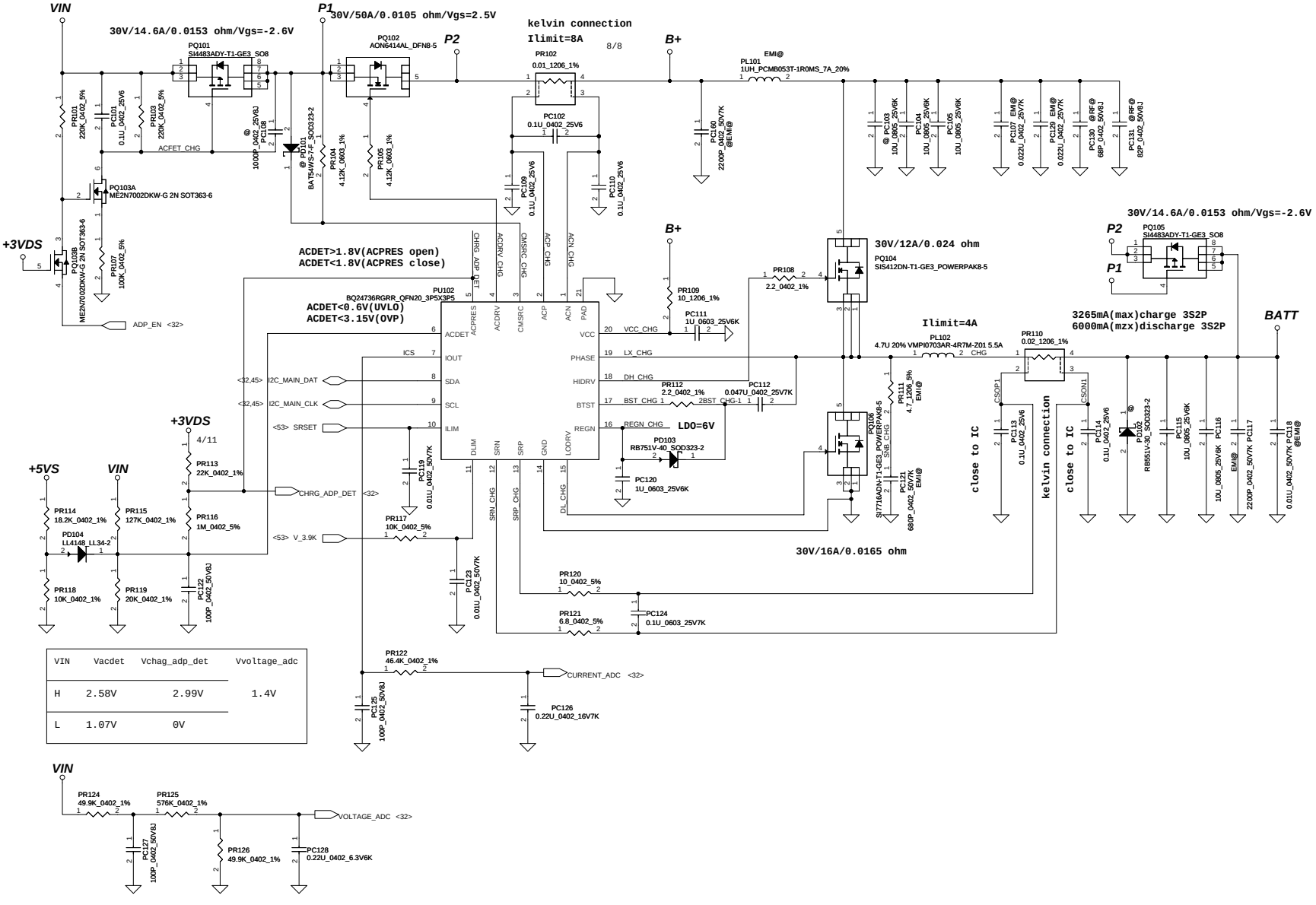
Compal Electronics, Inc.

Title: ***BATT Conn***

Size | Document Number: **LA-B181P** | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 45 of 62



VIN	Vacdet	Vchag_adp_det	Vvoltage_adc
H	2.58V	2.99V	1.4V
L	1.07V	0V	

Ilimit=20*(Vsrp-Vsrn)=20*Ich*Rch
up to Ilimit=1.6V(disable)
R=10m ohm I=8A
R=20m ohm I=4A
fs=750k

Iripple=Vin*D(1-D)/(fs*L),
D=0.5 (worst)
Iripple=1.418A
Isat(L)=Ichg+0.5*Iripple=4+0.5*1.418=4.709A

ILIM>1.6V disable
ILIM<75mV disable
ILIM>105mV enable

DLIM>1.1V disable
DLIM<870mV disable
DLIM>896mV enable(buck to boost)
default dischager current limit 4.096A

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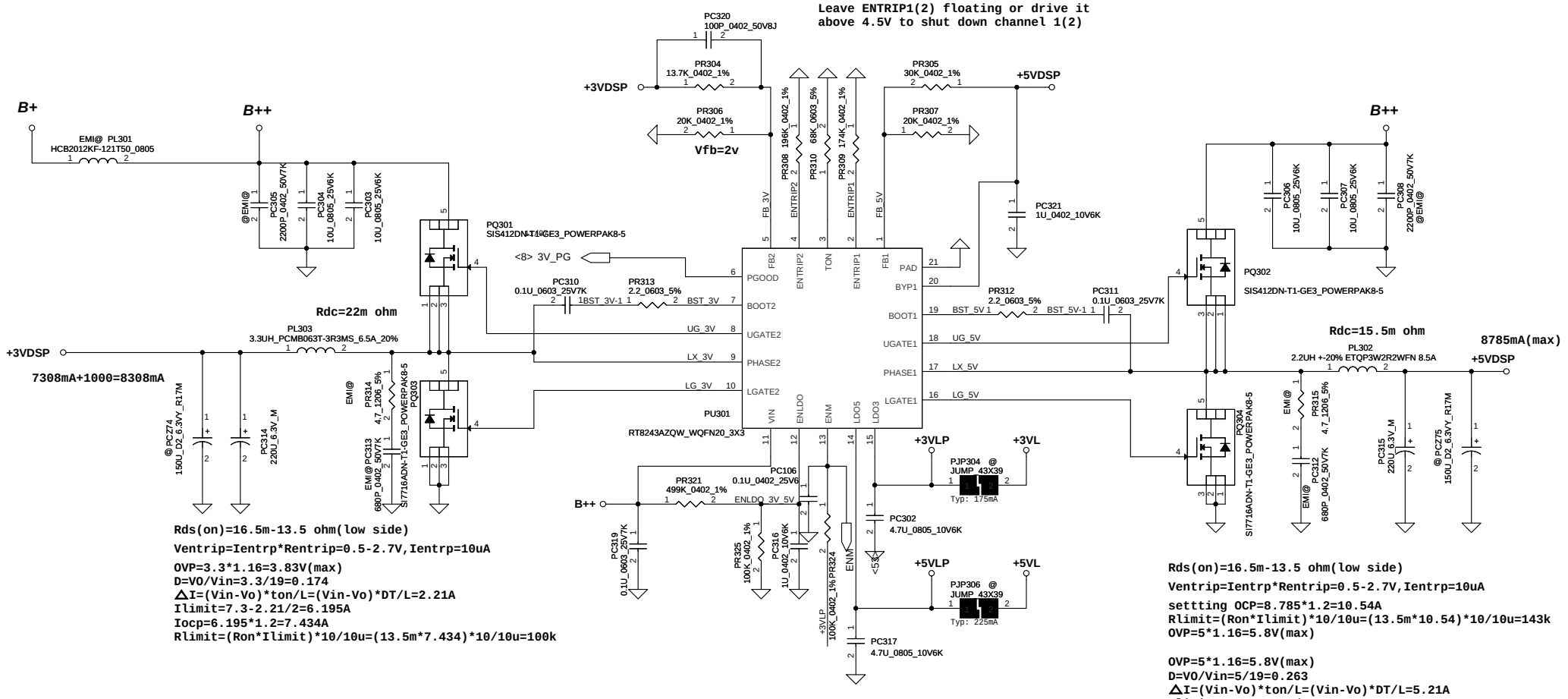
Title	CHARGER		
Size	Document Number LA-B181P		Rev 0.5
Date: Tuesday, March 25, 2014	Sheet 46 of 62		



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

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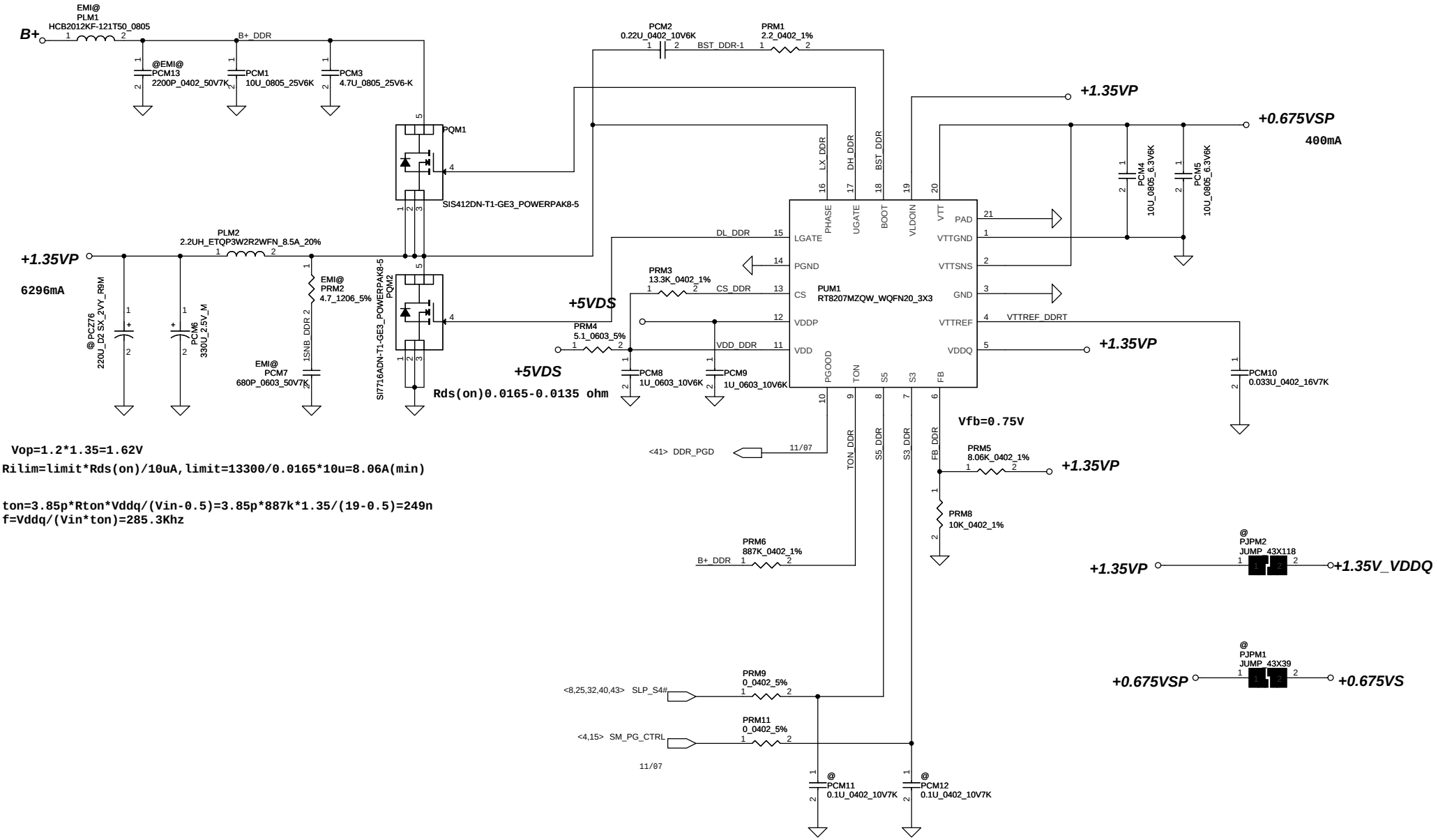
Compal Electronics, Inc.

Title: 3VDSP/5VDSP

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 47 of 62



Vop=1.2*1.35=1.62V

Rilim=limit*Rds(on)/10uA,limit=13300/0.0165*10u=8.06A(min)

ton=3.85p*Rton*Vddq/(Vin-0.5)=3.85p*887k*1.35/(19-0.5)=249n

f=Vddq/(Vin*ton)=285.3Khz

Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

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Compal Electronics, Inc.

Title: +1.35V/+0.675VS

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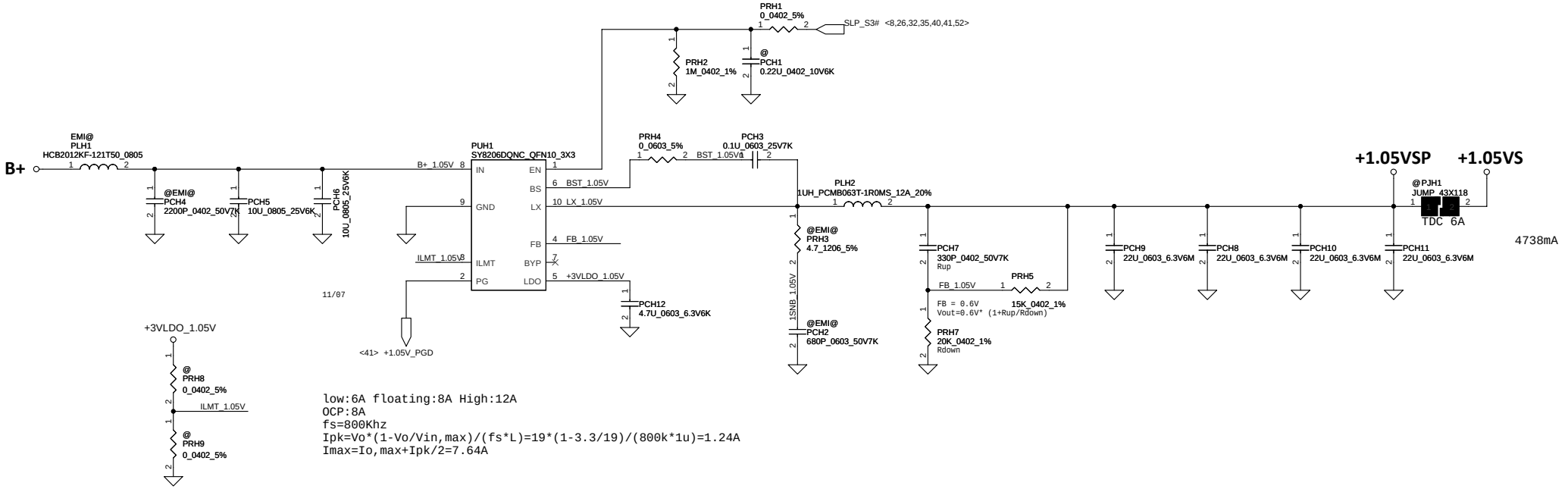

low:6A floating:8A High:12A
OCP:8A
fs=800Khz
Ipk=Vo*(1-Vo/Vin,max)/(fs*L)=19*(1-3.3/19)/(800k*1u)=1.24A
Imax=Io,max+Ipk/2=7.64A

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Issued Date	2013/09/09	Deciphered Date	2016/09/30

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Compal Electronics, Inc.

Title: ***+1.05VS***

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PRZ5:Vo-usr=1.7*(150/(150+9.53))=1.598V
Vusr=540mV
PRZ11:disable OSR&PT,Rosr=150k

PRZ10:setting fs R=150==>1Mhz

Ramp setting:
PRZ9=100K type:160mV
PRZ9>=150K type:40mV

boot voltage setting:
Vb-ram=1V==>2V
Vb-ram=0V==>1.7V
Vb-ram>1.525V==>0V

Iccmax=32A(15w),Iccmax=40A(28w)
IccTDC=10A(15w),IccTDC=16A(28w)
IccDyn=27A(15w),IccDyn=32A(28w)

OCP voatge seeting:
PRZ8=39K ==>18.9mV
Vimon=1.7V

Rp_n=10.74k Rcs(eff)=0.6m ohm
1.7V=10*(1+Rimon/39k)*0.6m*32,Rimon=345k

ALERT goes low,THERM=1.08V
VR_HOT goes low,THERM=1.1V

slew rate(15w,150K)=96mV/uS,slew rate(28w,100K)=84mV/uS
address selection(15w):1.7*100/(100+150)=0.68V
address selection(28w):1.7*100/(100+100)=0.85V

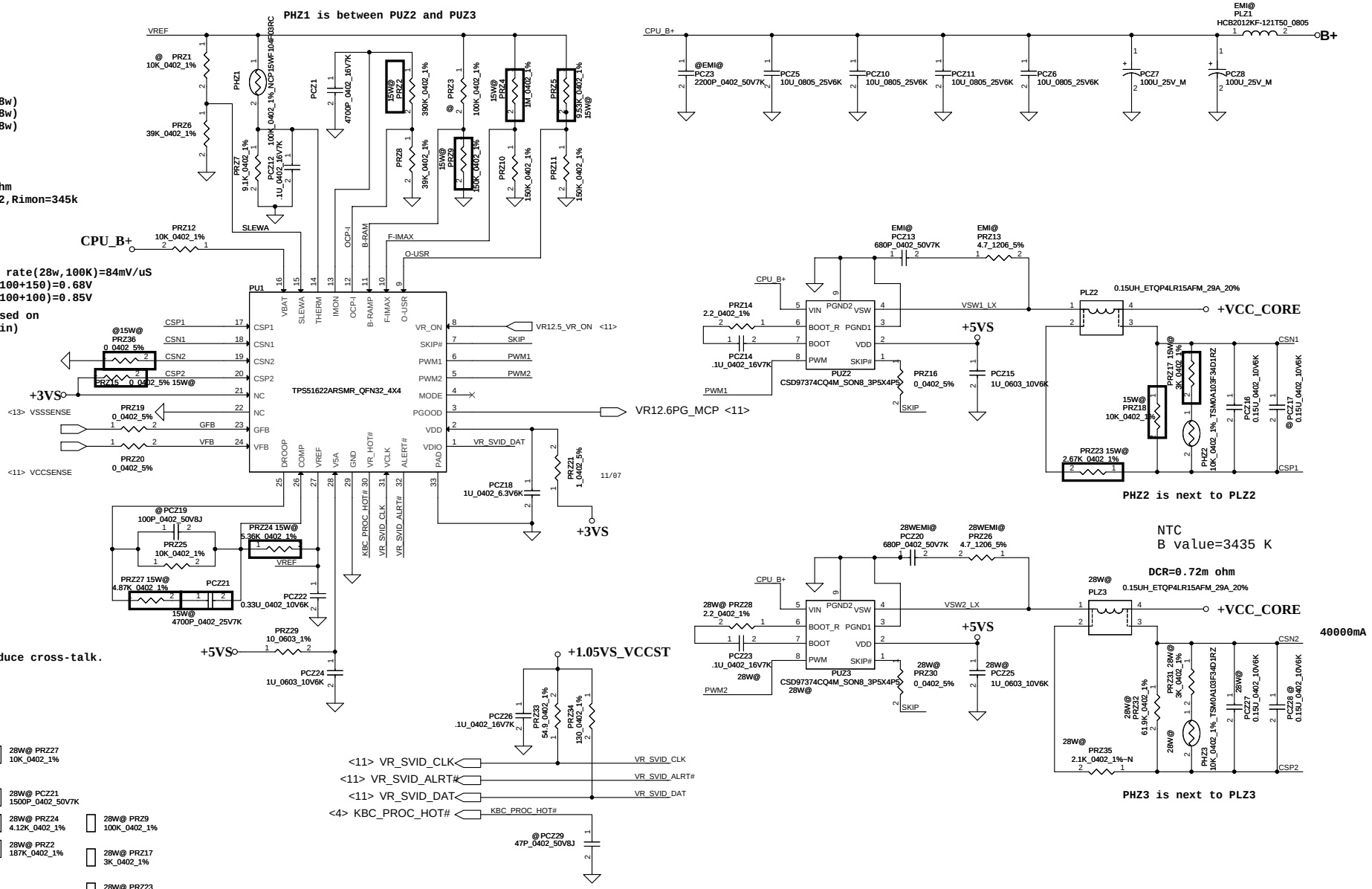
On-tome(ton):ON-time is fixed based on the input voltage (at the VBAT pin)

Vssense and Vccsense need to be difference pair

Droop:Error amplifier output.

ALERT between VCLK and VDIO to reduce cross-talk.

PHZ1 is between PUZ2 and PUZ3



PHZ2 is next to PLZ2

NTC
B value=3435 K

DCR=0.72m ohm

40000mA

PHZ3 is next to PLZ3

28W@ PRZ27 10K_0402_1%
28W@ PCZ21 1500P_0402_50V7K
28W@ PRZ24 4.12K_0402_1%
28W@ PRZ9 100K_0402_1%
28W@ PRZ2 187K_0402_1%
28W@ PRZ17 3K_0402_1%
28W@ PRZ4 806K_0402_1%
28W@ PRZ23 2.1K_0402_1%
28W@ PRZ5 280K_0402_1%
28W@ PRZ18 61.9K_0402_1%

not mount需特別注意(15w@,28w@)

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Compal Electronics, Inc.

Title: *+CPU_CORE*

Size: | Document Number: LA-B181P | Rev: 0.5

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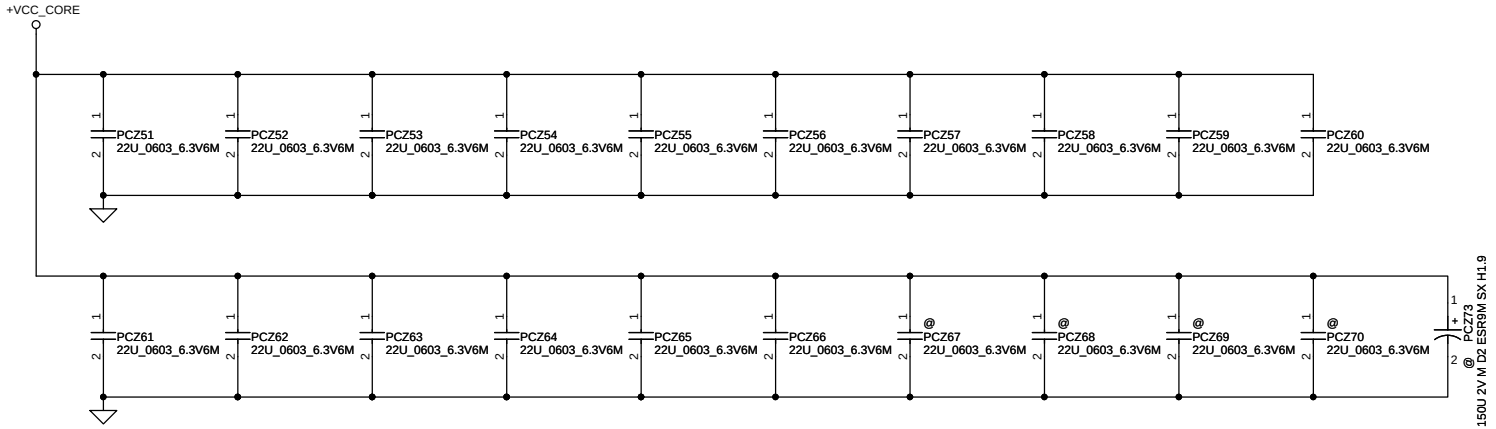

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Issued Date	2013/09/09	Deciphered Date	2016/09/30

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Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

Size | Document Number: **LA-B181P** | Rev: 0.5

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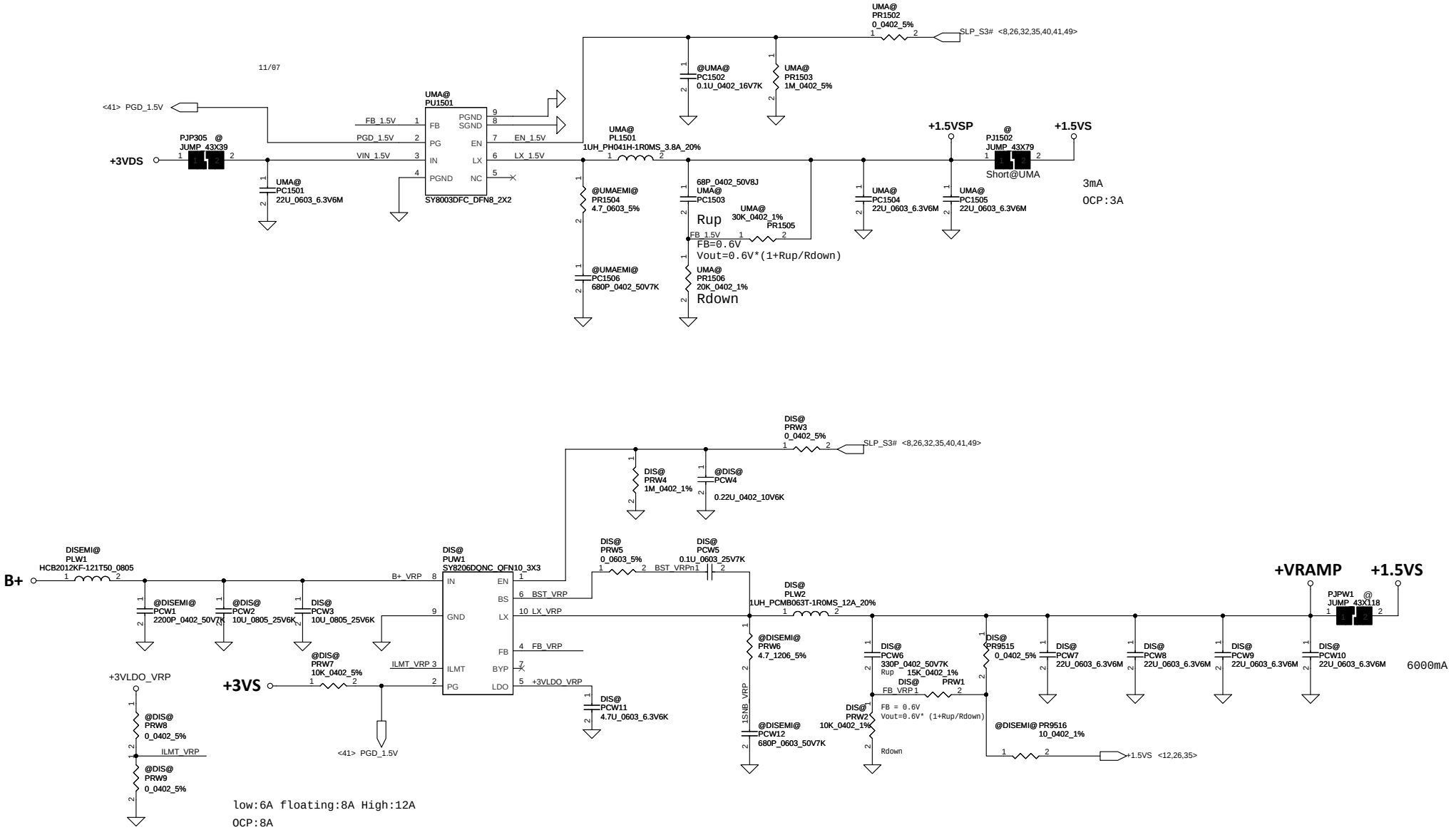

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Compal Electronics, Inc.

Title: *+1.5VS*

Size: | Document Number: LA-B181P | Rev: 0.5

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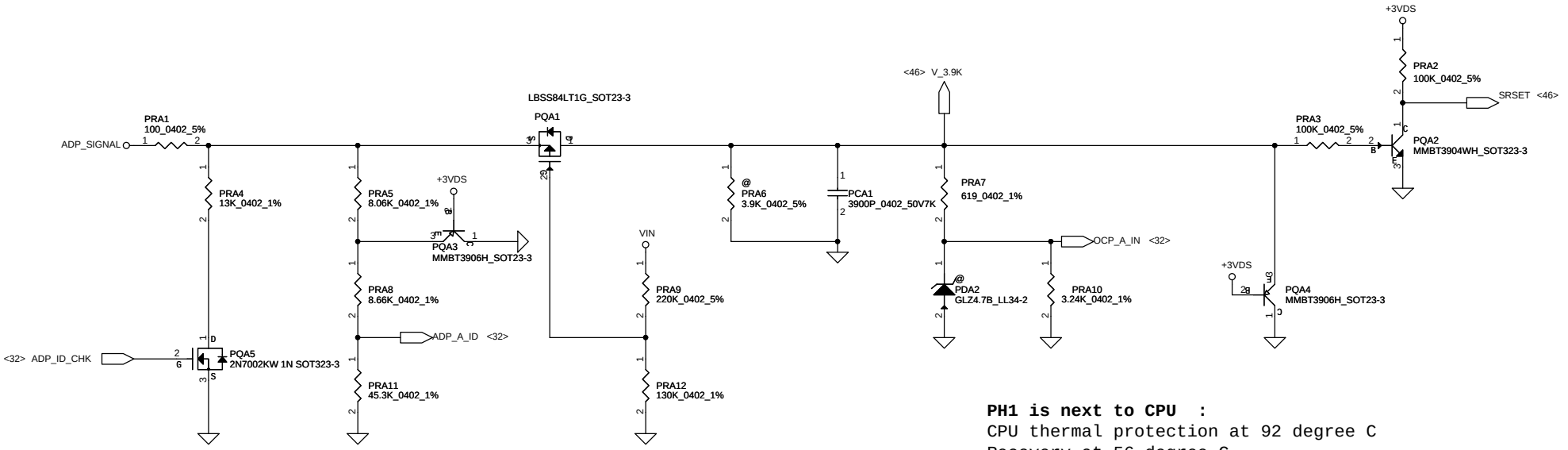
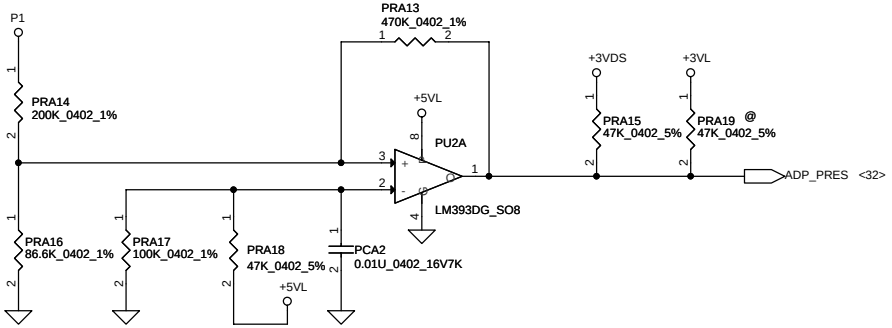
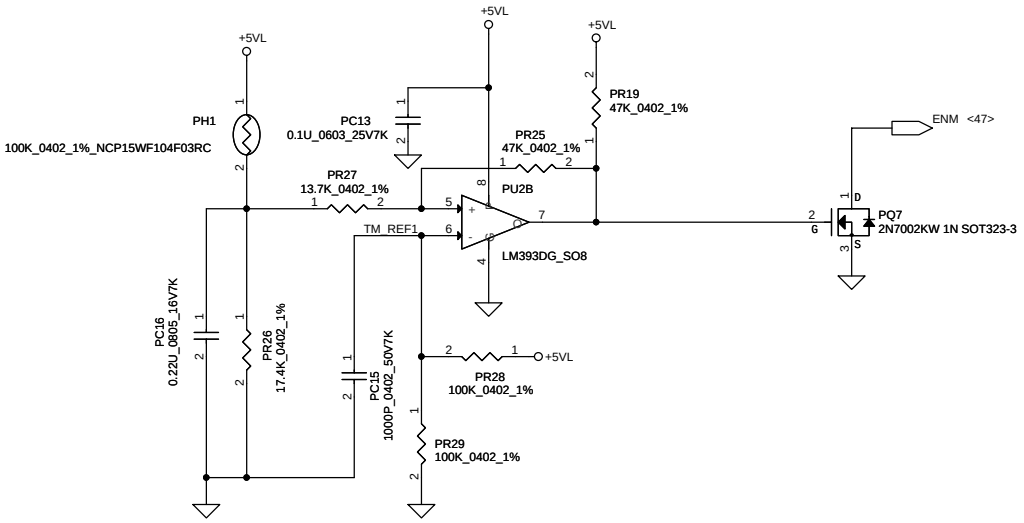


MEMO:PRA4 and PQA5 are not mount

PH1 is next to CPU :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





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Title	***ADP_OCP***		
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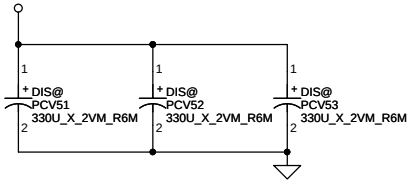
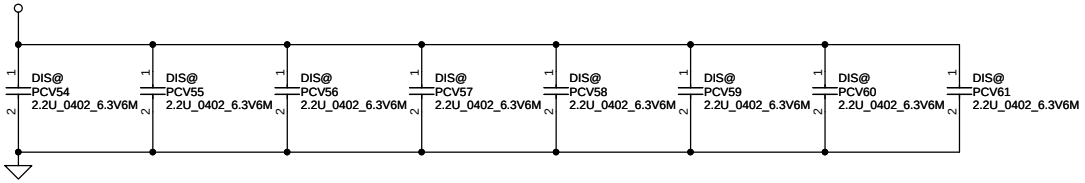
			Size: Document Number: LA-B181P Rev: 0.5
			Date: Tuesday, March 25, 2014 Sheet 54 of 60

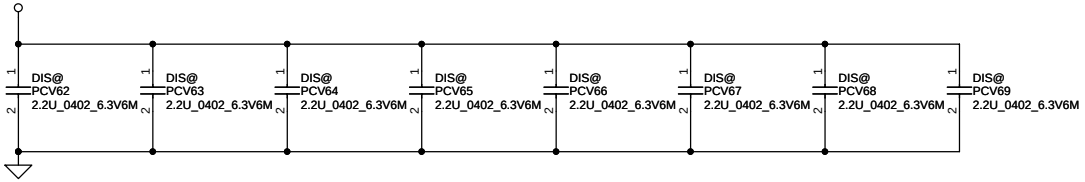
+VGA_CORE



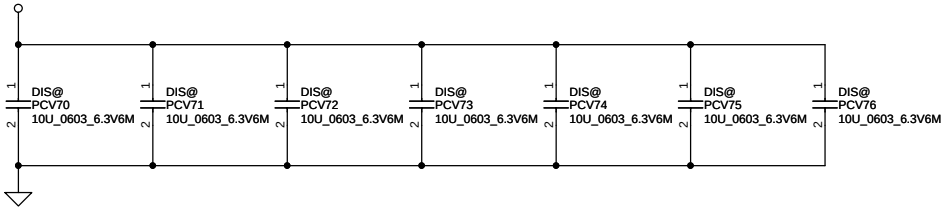
+VGA_CORE



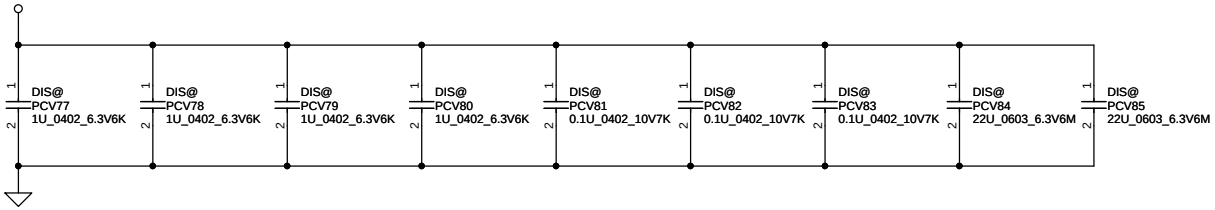
+VGA_CORE



+VGA_CORE



+VGA_CORE



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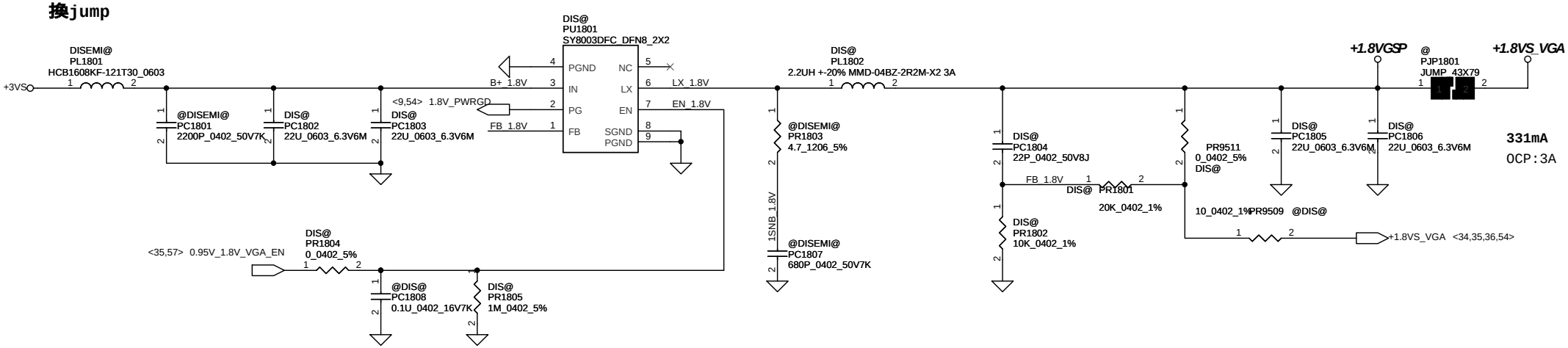
Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: *VGA CHIP DECOUPLING*

Size | Document Number: **LA-B181P** | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 55 of 62



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

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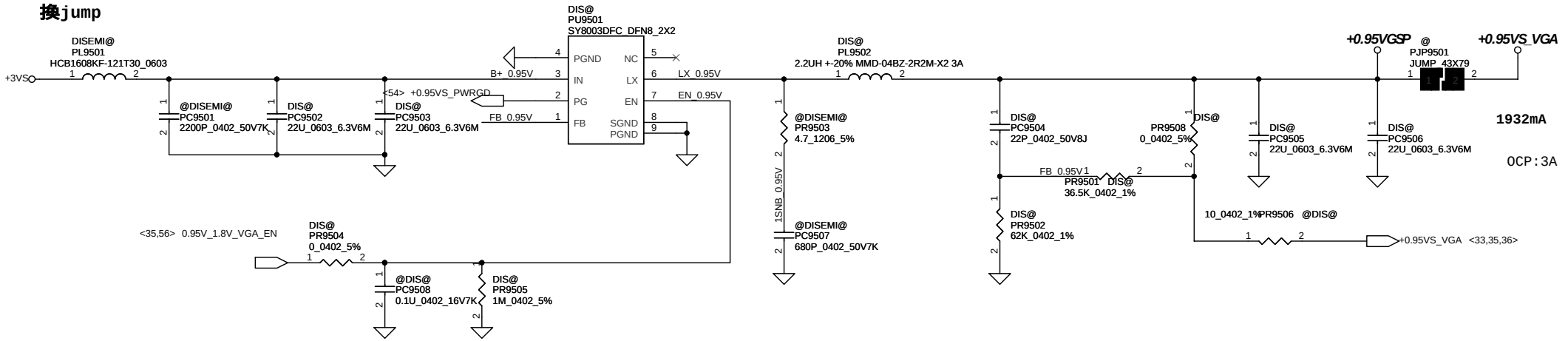
Compal Electronics, Inc.

Title: *+1.8VS_VGA*

Size: B | Document Number: LA-B181P | Rev: 0.5

Date: | Sheet 56 of 62



Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

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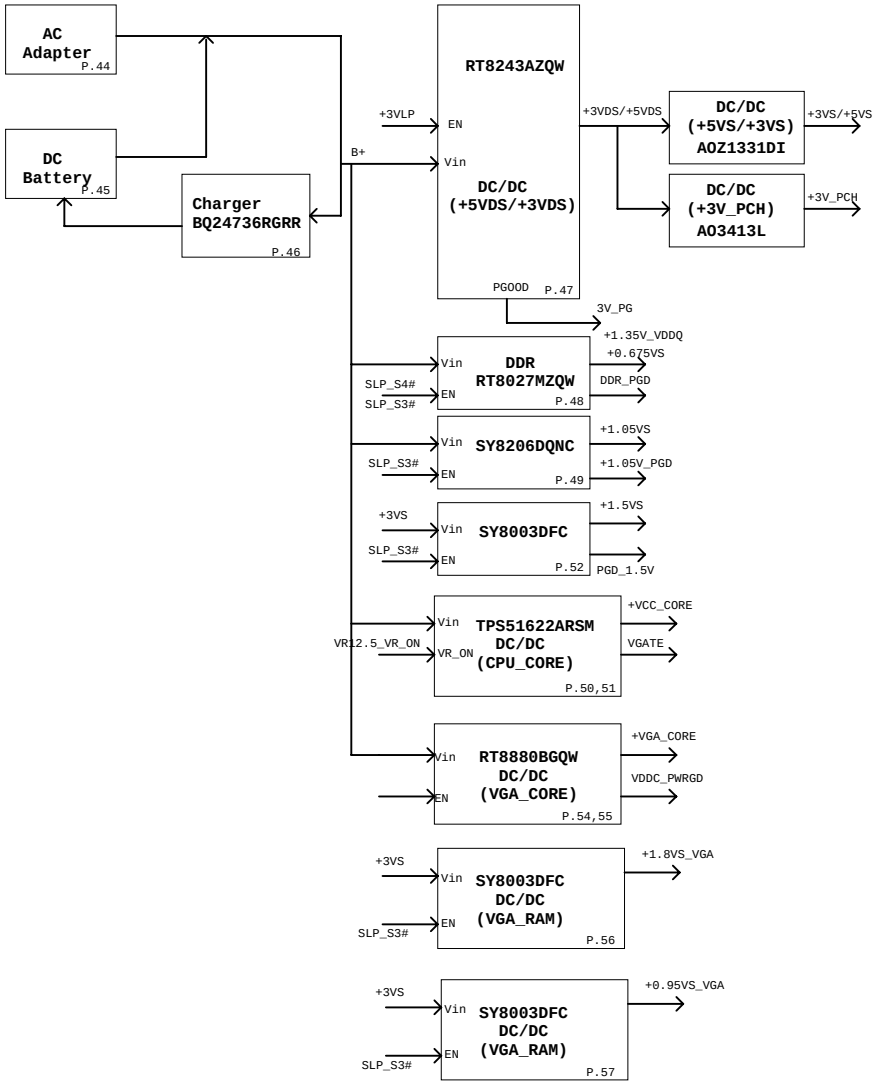
Compal Electronics, Inc.

Title: *+0.95VS_VGA*

Size: B | Document Number: **LA-B181P** | Rev: 0.5

Date: | Sheet 57 of 62



CPU DC/DC TPS51622ARSMR 50~51	
INPUTS	OUTPUTS
B+	VCC_VORE

SYSTEM DC/DC RT8243AZQW 47	
INPUTS	OUTPUTS
B+	3VDS/5VDS

SYSTEM DC/DC RT8207MZQW 48	
INPUTS	OUTPUTS
B+	1.35V_VDDQ 0.675VS

SYSTEM DC/DC SY8206DQNC 49	
INPUTS	OUTPUTS
B+	1.05VS

SYSTEM DC/DC SY8003DFC 52	
INPUTS	OUTPUTS
B+	1.5VS

SYSTEM DC/DC RT8880BGQW 54~55	
INPUTS	OUTPUTS
B+	+VGA_CORE

SYSTEM DC/DC SY8003DFC 56	
INPUTS	OUTPUTS
B+	+1.8VS_VGA

SYSTEM DC/DC SY8003DFC 57	
INPUTS	OUTPUTS
B+	+0.95VS_VGA

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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Compal Electronics, Inc.

Title: *Power Block Diagram*

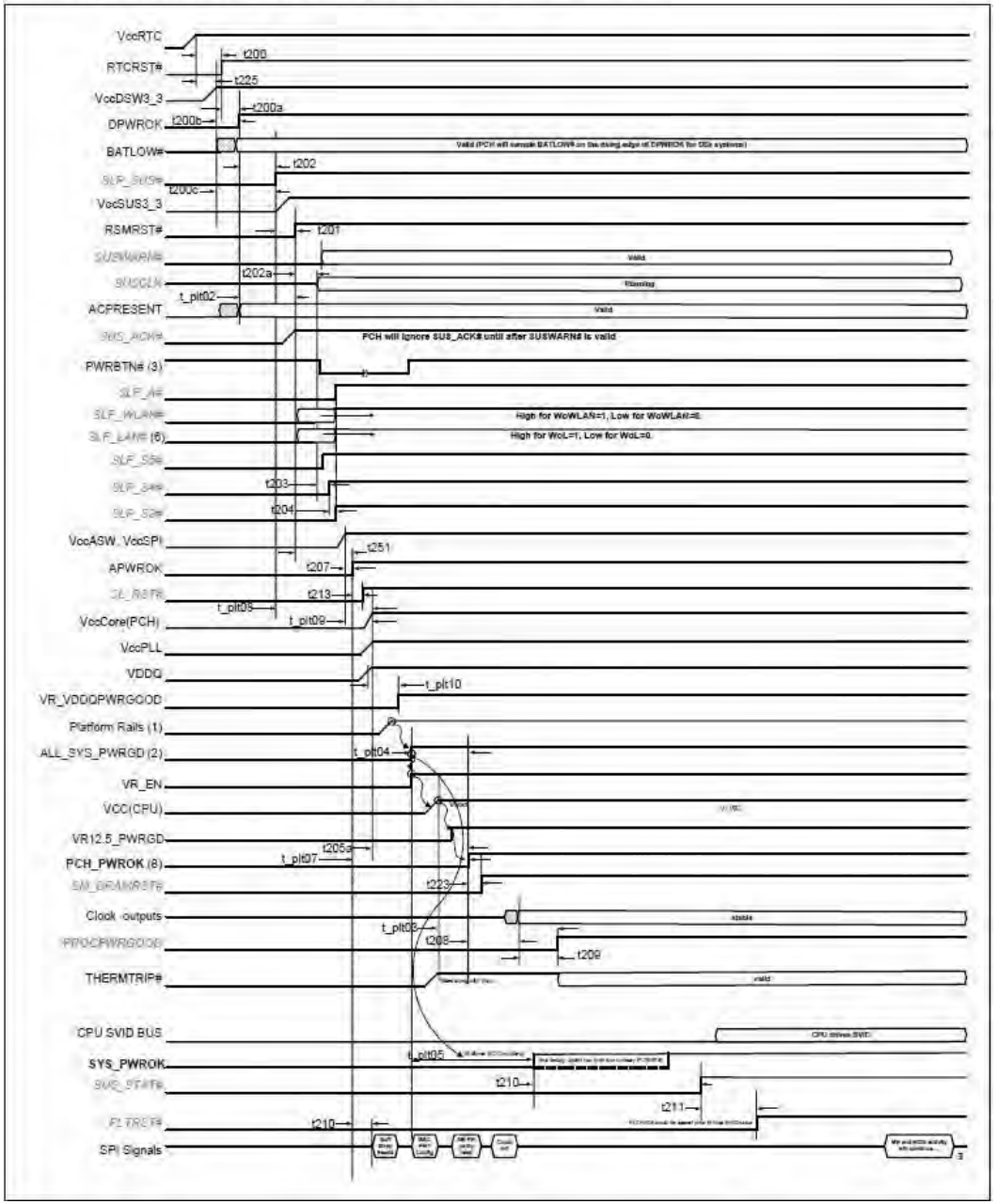
Size: Document Number: LA-8181P

Rev: 0.5

Date: Tuesday, March 25, 2014 Sheet 58 of 60

Power ON Sequence

Timing Diagram for G3 to S0/M0 [Deep Sx Platform]



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: Power ON Sequence

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Size	Document Number	Rev
C	LA-B181P	0.5

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Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	20131030		Delete 1.PQ307 2.charger air line power circuit 3.change AON7506 to SI7716(PQ106) 4.change NDS0610 to LBSS84L 5.change AON7506 to SI7716 6.change 47U 6.3V to 22U 6.3V (PCH8,PCH9) 7.PR9512 mount	1.customer request 2.customer request 3.customer common part 4.compal change 5.customer common part 6.vender reveiw	DB0 DB0 DB0 DB0
2	20131031		1.10U_0805_25V==>2200p_0402_50V not mount(PC160) 2.PC107,PR111,PC121,PC305,PR314 PC313,PC308,PR315,PC312,PCH4,PCZ3,PRZ13,PCZ13 PCZ20,PCZ26,PCW1,PCV4,PRV70,PCV107 3.change 147K_0402_1% to 237K_0402_1% (PRV34) change 560P_0402_50V7K to 470P_0402_50V7 (PCV88) change 10.7K_0402_1% to 22.6K_0402_1%(PRV47) change 9.76K_0402_1% to 5.6K_0402_1%(PRV51) change 15K_0402_1% to 19.1K_0402_1%(PRV55) change 910K_0402_5% to 20.5K_0402_1%(PRV75) change 910k_0402_1% to 910_0402_1%(PRV53) change 3.48K_0402_1% to 3.4K_0402_1%(PRV69) change 910k_0402_1% to 910_0402_1%(PRV77) 4.remove PR9510,PR9512,PR9514,PR9513 5.remove PC318,PRH10,PRW10,PCW13 6. PRH8,PRW8 not mount 7.22u/0805 6.3V to 22u/0603 6.3V PC1504,PC1501 PC1505,PC1802,PC1803,PC1805,PC1806,PC9502,PC9503, PC9505,PC9506,PCH9,PCH10,PCH11,PCH8 8.0.22U_0402_6.3V6K to 0.22U_0603_50V7K (PC128)	1.EMI feedback 2.EMI feedback 3.power vender feedback 4.power change fb sense 5.for compal module design 6.current limit design	DB0 DB0 DB0 DB1 DB1 DB1 DB1 DB1 DB1 SI1 SI1 SI1
3	20131101		1.remove PRW11	1.HW request	
4	20131112		1.not mount PRW7 2.change 0_0402_1% to 0_0402_5%(PR1502,PR1804, PR9504,PR9508,PR9511,PR9515)	2.AMD request	
5	20131202		1.not mount PRZ36,PRV32 and PCV86 2.PC128 change 0.22U_0603_25V to 0.22U_0402_6.3V6K 3.add PD16,PRV43 4.add PRV45,PRV48,PCV99 and PRV50	1.PWR request 2.PWR request 3. customer request 4.richtek request	SI1 SI1 SI2
					SI2

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

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Compal Electronics, Inc.			
Title: PIR List			
Size: B	Document Number: LA-B181P		Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 60 of 62		

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
6	20131210		add PRV78 1K_0402_1% PRV62 5.76K_0402_1% PRV64 10K_0402_1% PRV80 1K_0402_1% PRV79 10K_0402_1% PRV52 137K_0402_1%	RITCHTEK issue request	DB0 DB0 DB0 ~~DB0~~
	20131221		PRM2 Change 4.7_1206_5% to 0_1206_5% PCM7 Change 680P_0603_50V7K to 1000P_0603_50V7K PR314 not mount==>mount PC313 not mount==>mount PR315 not mount==>mount PC312 not mount==>mount PCZ13 not mount==>mount PRZ13 not mount==>mount PCZ20 not mount==>mount(28W) PRZ26 not mount==>mount(28W)	EMI request	DB0 DB0 DB0 DB1 ~~DB1~~
	20131226		PRV31 Change 10_0402_1% to 1_0402_1% PRV34 Change 127K_0402_1% to 84.5K_0402_1% PRV47 Change 22.6K_0402_1% to 7.32K_0402_1% PRV51 Change 5.6K_0402_1% to 12.4K_0402_1% PRV55 Change 19.1K_0402_1% to 14K_0402_1% PRV75 Change 20.5K_0402_1% to 2.8K_0402_1% PRV77 Change 910_0402_1% to 1.3K_0402_1% PRV53 Change 910_0402_1% to 1.3K_0402_1% PC128 Change 0.22U_0603_6.3V to 0.22U_0402_6.3V	RITCHTEK issue request	DB1 DB1 DB1 DB1 SI1
	20140102		PRM2 Change 0_1206_5% to 4.7_1206_5% PCM7 Change 1000P_0603_50V7K to 680P_0603_50V7K PUV1 change RT8880BGQW to RT8880CGQW	EMI request RITCHTEK request	SI1 ~~SI1~~
	20140103		PR14,PQ2 and PR13 are not mount. PR11 Change 330_0402_1% to 680_0402_1%	Customer request	
	20140106		PRV80 mount==>not mount PRV79 not mount==>mount	RITCHTEK issue request	
	20140213		add PC8,PC9 and PC10 mount PR111,PC121,PC107 and PC129 PC107 2200P_0402_50V7K==>0.022_0402 25V PC129 0.1U_0402_50V7K==>0.022_0402_25V	EMC request EMC request	
	20140214		add PC161 2200P_0402_50V7K not mount	EMC request	SI1 SI1 SI2 SI2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: PIR List
Size: B	Document Number: LA-B181P		Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 61 of 62		

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ZPL40/50/70 from DB to DB-R LA-B181P REV:0.1 -> 0.2 Modify <2013.11.28.~ 2013.12.03>

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.2	1	11/28	CKT, LAYOUT	6	-Design issue	-Change RC222 pin 1 connection from +3VS to +5VS
0.2	2	11/28	CKT, LAYOUT	7	-Follow CHICLET	-Move TPM LPC CLK from port 0 to port 1
0.2	3	11/28	CKT	8	-DGPU_PWR_EN voltage level uncorrect issue	-Uninstall RC125
0.2	4	11/28	CKT, LAYOUT	9	-DGPU power on sequence	-Change RC121 to 100K and add CC127 to timing delay.
0.2	5	11/28	CKT, LAYOUT	18	-Footprint uncorrect issue	-Modify UT6 footprint to SC70-5
0.2	6	11/28	CKT, LAYOUT	21	-No used.	-Remove CLK_PCI_DEBUG from JMINI1 pin 19
0.2	7	11/28	CKT	23	-Q35 can't turn on issue	-Uninstall RL26
0.2	8	11/28	CKT	30	-Follow HP BIOS code request	-Uninstall R124
0.2	9	11/28	CKT, LAYOUT	32	-Avoid leakage issue.	-Swap Q88 pin 1 and pin 3
0.2	10	11/28	CKT, LAYOUT	32	-Footprint uncorrect issue	-Modify C187 footprint to 0402 package
0.2	11	11/28	CKT, LAYOUT	33	-Design issue	-Swap GPU PEG RX bus P/N signal and CV1~CV8 change to 0.22u
0.2	12	11/29	CKT, LAYOUT	28	-Current limit	-Add R660
0.2	13	11/29	CKT, LAYOUT	30	-Vendor request	-U13 pin 6 add external 4.7K PU to +3VS_TPM
0.2	14	11/29	CKT	32	-Follow CHICLET	-Change R255, R257, and R493 to 10Kohm -Delete QC12 and add buffer U20 and U21.
0.2	15	12/02	CKT, LAYOUT	6	-Follow CHICLET	QC8.3 net name from HDA_SDOUT_AUDIO change to HDA_SDOUT
0.2	16	12/02	CKT, LAYOUT	32	-Follow CHICLET	add R101, R102, R104, R105, R106
0.2	17	12/02	CKT, LAYOUT	23	-leakage issue and FAR suggest	1.swap QL2 pin 1 and pin 3 2.install RL40 3.Reserve 2 resistor (RL48, RL49) connection QL2.2 to +3VS and +LAN_VDD_3V3.
0.2	18	12/02	CKT, LAYOUT	34	-Follow 2013 RRR	-Add D14
0.2	19	12/02	CKT	35	-DGPU power on sequence	-Uninstall R5076, R5074
0.2	20	12/03	CKT, LAYOUT	40	-Follow CHICLET	-change +1.05VS_MODPHY switch circuit

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.2 -> 0.3 Modify <2013.12.04~ 2013.12.17>

0.3	1	12/04	CKT, LAYOUT	29	-Follow 2013 RRR	-update FAN control circuit delete Q4108, R5080 and add U2, C31
0.3	2	12/05	CKT	35	-DGPU power on sequence	-C4816 from 0.01u change to 0.022u
0.3	3	12/05	CKT	9	-DGPU power on sequence	-Change RC121 to 0ohm and uninstall CC127 (BIOS code control timing)
0.3	4	12/05	CKT	10, 33	-For PCIe Gen2	-change CC89, CC90, CC91, CC92, CC93, CC94, CC95, CC96, CV1, CV2, CV3, CV4, CV5, CV6, CV7, CV8 from 0.22u to 0.1u
0.3	5	12/06	CKT	12	-Follow CHICLET	-Change RC174 from 5.11ohm to 0ohm
0.3	6	12/06	CKT	11	-Follow INTEL schematic	-Change RC156 from 110ohm to 130ohm install
0.3	7	12/06	CKT, LAYOUT	29	-Platform ID identify	-add R82, R86
0.3	8	12/06	CKT, LAYOUT	32		-reserve R136, R137 co-lay with U20, U21
0.3	9	12/06	CKT, LAYOUT	40		-reserve R135 co-lay with Q185
0.3	10	12/09	CKT, LAYOUT	43	-No leakage issue	-remove Q57
0.3	11	12/09	CKT	26	-Follow CHICLET	-RA36 from 22ohm change to 33ohm
0.3	12	12/09	CKT, LAYOUT	17	-Follow INTEL schematic	-Install CD52, CD53, CD54, RD11, RD12, RD19 and re-placement RD7, RD8, RD15
0.3	13	12/09	CKT, LAYOUT	11	-Follow INTEL schematic	-Re-placement RC154
0.3	14	12/09	CKT, LAYOUT	12	-Follow INTEL schematic	-Add RC183, CC47, RC189, CC75
0.3	15	12/10	CKT, LAYOUT	10	-For WWAN , Touch share USB port	-Add R138, R139
0.3	16	12/10	CKT, LAYOUT	4	-Follow CHICLET	-Add C32
0.3	17	12/11	CKT, LAYOUT	8	-Follow INTEL schematic	-reserve RC330
0.3	18	12/11	CKT, LAYOUT	21	-solve SIM card can't detect issue	-delete R5079 , Q4107 and add C2
0.3	19	12/13	CKT, LAYOUT	9	-Follow Runt	-R103 change to test point T184
0.3	20	12/13	CKT	8	-solve DGPU power issue	-Install RC125
0.3	21	12/13	CKT, LAYOUT	21	-Follow Runt	-Q90 , Q4113 from two single MOS change to daul MOS (Q90)
0.3	22	12/13	CKT, LAYOUT	22	-ODD power issue	-Add Q63
0.3	23	12/13	CKT, LAYOUT	23	-LAN power issue	-delete JHW1 , RL26
0.3	24	12/13	CKT, LAYOUT	21	-no need	-delete R205 , C292
0.3	25	12/13	CKT	25	-For V drop test	-C1572 from 100u change to 150u
0.3	26	12/13	CKT, LAYOUT	9	-Hp request	-ODD_DA# form GPIO14 change to GPIO3
0.3	27	12/13	CKT, LAYOUT	21	-For GPIO initial status	-add R91
0.3	28	12/14	CKT, LAYOUT	12	-solve power ripple	-add CC77 , CC78 , CC79
0.3	29	12/16	CKT, LAYOUT	9	-reserve for MPHY sequence	-add RC377

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.3 -> 0.4 Modify <2013.12.18~ 2013.12.25>

0.4	1	12/20	CKT	9	-Follow HP request	-Install RC272, RC273
0.4	2	12/20	CKT, LAYOUT	15	-Follow Intel PDG	-Remove RD26, Install RD21
0.4	3	12/20	CKT, LAYOUT	16	-Follow Intel PDG	-Unnstall CD52, CD53, CD54, RD11, RD12, RD19 and re-placement RD7, RD8, RD15
0.4	4	12/20	CKT, LAYOUT	19	-Follow Vendor request	-Reserve RG5
0.4	5	12/20	CKT	19	-Follow HP request	-Change R82, R86 to 0 ohm
0.4	6	12/20	CKT	20	-Follow Intel PDG	-Change RP3 and RP4 to 470 ohm
0.4	7	12/20	CKT	21	-Compal Request	-Install R91
0.4	8	12/20	CKT, LAYOUT	22	-Customer modify GPIO table.	-Remove Q84, R954. Change JODD1 pin 11 netname to ODD_DA#
0.4	9	12/20	CKT	23	-Prepare leakage issue when S3, S5	-Uninstall RL40, QL2, RL49, RL48 install RL34
0.4	10	12/20	CKT	24	-Vendor Request	-Reserve RA40, U4101 pin 37 add RT57 10K PU to +5VS
0.4	11	12/20	CKT	31	-Vendor Request	-Remove R1363, R1365, R1367, C421, C423, C414, L31, L32, L34, R1364, R1366, and R1368. Modify CRT pi filter
0.4	12	12/20	CKT, LAYOUT	40	-Follow Compal common design	-Modify MPHY Power circuit
0.4	13	12/23	CKT, LAYOUT	30	-Follow RF team request	-Install C80, C556, C81, C558 -Reserve C90, C564, C91, C565, C92, C566, C93, C567, C95, C569, C110, C578, C111, C579, C108, C576, C82, C559, C83, C560, C84, C561, C86, C562, C89, C563, C94, C568, C96, C571, C112, C580, C109, C577, C106, C574, C97, C572, C105, C573, C130, C581, C131, C582, C132, C583, C133, C584, C134, C585, C135, C586, C136, C587, C137, C588, C138, C589
0.4	14	12/24	CKT, LAYOUT		-Follow ESD team request	-Install C113, C127 -Reserve C114, C115, C116, C121, C123, C124, C128, C129

ZPL40/50/70 from SI to PV-1 LA-B181P REV:0.3 -> 0.4 Modify <2014.02.05~2014.>

0.5	1	02/05	CKT	21	-Double pull hugh	-RN3 change to @
0.5	2	02/05	CKT	18, 19	-For LVDS SKU	-R163, RG3 change to LVDS@
0.5	3	02/05	CKT	19	-For eDP SKU	-R172 change to eDP@
0.5	4	02/05	CKT	19	-For Lid Switch issue	-R166, R175 change to 3.3K
0.5	5	02/05	CKT, LAYOUT	22	-For ODD issue	-add R448, reserve C151
0.5	6	02/05	CKT, LAYOUT			-1. QA2, QA3 combine to dual mos QA2A, QA2B 2. Q81, Q182 combine to dual mos Q81A, Q81B 3. Q86, Q87 combine to dual mos Q86A, Q86B 4. Q63 change to Q63A, Q63B 5. Q4112, Q4114 combine to dual mos Q4112A, Q4112B
0.5	7	02/10	CKT, LAYOUT	35	-For GPU Power Sequence	-add D15 and move R5075, C4819
0.5	8	02/10	CKT, LAYOUT	28	-Follow ESD team request	-add C594, C595, C596
0.5	9	02/10	LAYOUT	31		-Move U4101 circuit close to JCRT
0.5	10	02/11	CKT, LAYOUT	40	-SLG59M1470VTR is single source issue	-modify U44 circuit
0.5	11	02/12	CKT	33	-Improve VGA_PWRGD signal quality	-R5094 from 8.25K change to 0ohm
0.5	12	02/13	CKT, LAYOUT	11, 19	-Follow RF team request	-add C139, C140, C421
0.5	13	02/14	CKT, LAYOUT		-Follow HP request	-1. FPR_OFF from GPIO11 change to GPIO65 2. change JAUDIO1.16 from +3V_PCH to +3VS 3. disconnect EC pin125 and CPU pinAJ5 rename EC pin125 "PCH_PCIE_WAKE#" to "EC_GPIO25" and add R249 pull up to +3VDS 4. RN13 un-install 5. connector EC pin103 to JMINI1 pin1 (WLAN_WAKE#), JMINI2 pin15 change to NC 6. connector EC pin105 to CPU pinAJ5 (PCH_PCIE_WAKE#) 7. change RN3 pull up power rail from +3VS_WLAN to +3VDS and install RN3 8. add JP4102 between +3VDS and +3V_WWAN

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